Curriculum vitae

PERSONAL INFORMATION

Ioannis Messaris

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WORK EXPERIENCE

01/12/2013–25/01/2014

Researcher - Engineer

Helic Inc., Athens (Greece)

- Investigation of the merits of TG-FinFET transistor devices versus traditional planar technologies by comparisson in digital circuits in terms of delay, power consumption and area.

- The work was conducted within the COOPERATION Program of the General Secretariat for Research and Technology under contract 09ΣΥΝ-42-998, which was cofinanced by the European Regional Development Fund and Greek National Funds.

01/02/2014–30/11/2014

Researcher - Engineer

ELKE AUTH, Thessaloniki (Greece)

- Development of analytical digital cell models for the Nan Gate open cell library.

- Relevant work package title: "Continuous Transistor Sizing Toolset for nanoscale IC optimization"

- The work was conducted within the COOPERATION II Program of the General Secretariat for Research and Technology under contract 11ΣΥΝ-5-719, which was cofinanced by the European Regional Development Fund and Greek National Funds.

01/12/2014–Present

Researcher - Engineer

ELKE AUTH, Thessaloniki (Greece)

- Development of analytical compact reliability models under hot-carrier electrical stress.

- Lifetime prediction of TG-FinFET devices.

- Adaptation of the implemented models in modern simulating environments.

- Relevant work package title: "Compact modelling of emerging NANO-scale multi-gate MOSFETs and reliability simulation tool for robust analog & mixed signal design facilitation

- This work was supported by ARISTEIA II (project 4154) of the Greek General Secretariat for Research and Technology, co-funded by the European Social Fund and national funds.

EDUCATION AND TRAINING

2001–2007

Physics degree

Aristotle University of Thessaloniki, Thessloniki (Greece)

2009–2012

MSc in Electronic Physics

Aristotle University of Thessaloniki, Thessaloniki (Greece)

- Compact model implementation of TG-FinFET device in the Verilog-A hardware description language

PERSONAL SKILLS

Mother tongue(s) Greek

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C2	C2	C2	C2	C2
Certificate of Proficiency in English (ECPE) - University of Michigan					

Levels: A1 and A2: Basic user - B1 and B2: Independent user - C1 and C2: Proficient user
Common European Framework of Reference for Languages

Computer skills

- Microsoft Windows
- Linux
- Microsoft Word/Excel/Powerpoint
- Origin
- Mathematica
- HSPICE
- Cadence

ADDITIONAL INFORMATION

Publications

- I. Messaris, F. Karagiorgos, P. Chaourani and S. Nikolaidis, "Static gate power consumption model based on power contributors," Proceedings of DCIS 2014 Conference, Madrid, Nov 2014.
- P. Chaourani, I. Messaris, N. Fasarakis, M. Ntogramatzi, S.Goudos and S. Nikolaidis, "An analytical model for the CMOS inverter," Proceedings of PATMOS 2014 Workshop, Mallorca, Sept 2014.
- D.H. Tassis, I. Messaris, N. Fasarakis, S. Nikolaidis, G. Ghibaudo and C. Dimitriadis, "Variability analysis - Prediction method for nanoscale triple gate FinFETs," Proceedings of MIEL 2014 Conference, Madrid, May 2014.
- D.H. Tassis, I. Messaris, N. Fasarakis, A.Tsormpatzoglou S. Nikolaidis, G. Ghibaudo and C. Dimitriadis, "Variability of Nanoscale Triple Gate FinFETs," Proceedings of ICECS 2014 Conference, Marseille, Dec 2014.
- Ch. Galani, A. Tsormpatzoglou, P. Chaourani, I. Messaris and S. Nikolaidis, "A study for replacing CMOS gates by equivalent inverters," Accepted for submission for CPE 2015 Conference, Lisbon, Jun 2015.

Presentations

- "Static gate power consumption model based on power contributors," Presentation at DCIS 2014 Conference, Madrid, Nov 2014