Cirriculum Vitae

Lampros Mountrichas

Physicist – M.Sc. Electronics Engineering

Date of birth	9/11/1983
Place of birth	Athens, Greece
Marital status	Single
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PROFESSIONAL EXPERIENCE

ARISTOTLE UNIVERSITY OF THESSALONIKI

Researcher **9/2009 - Present**

Design and layout of:

- High-Speed Divider (Prescaler and digital Divider), for an E-band 71GHz-86GHz Transceiver in 65nm CMOS. [Project Leader – Ceragon Hellas]
- 1.7-GS/s 6-bit Flash ADC for a 60GHz Transceiver in 90nm CMOS [Theta Microelectronics]
- 1.7-GS/s 6-bit current steering DAC for a 60GHz Transceiver in 90nm CMOS. [Theta Microelectronics]
- 10ppm Trimmable Bandgap Voltage reference in 180nm CMOS [Theon sensors]
- Rail-to-Rail 14-bit integrating A/D converter in 180nm CMOS [Theon sensors]

Supervision and co-design of:

- NMOS Bulk Voltage Trimming Offset Calibration Technique for a 6-bit 5GS/s Flash ADC, in 90nm CMOS
- Layout design of a low noise LDO, in 180nm CMOS
- Analog part of a low speed ADC. Design of the digital control and SPI block, in 180nm CMOS

LARCO – GMMSA

Physicist – Internship **7/2004 – 9/2004**

- Evaluation of the two possible causes of malfunction (stuck and broken hammers) for a stone crusher.

RELEVANT SKILLS

Electronic Design Automation Tools
Cadence Virtuoso suite, Cadence Encounter RTL Compiler, Cadence Encounter Digital Implementation , ModelSim, Nclaunch

Hardware Description Languages
VHDL (Basic Knowledge)

Computer Programming Languages (Basic Knowledge)
Visual Basic, Assembly, Labview, Matlab

PUBLICATIONS

Journals

L. Mountrichas, S.Siskos, "A high-speed offset cancelling distributed sample-and-hold architecture for flash A/D converters", Microelectronics Journal, July 2013

A.Voulkidou, **L.Mountrichas**, S.Siskos "An Adaptable 14-Bit Dual Slope ADC with Wide Input Range", Procedia Engineering, Volume 47, 2012

V. Kalenteridis, **L. Mountrichas**, S. Vlassis, S. Siskos, "A CMOS linear-in-dB VGA and AGC loop for telecommunication applications", Microelectronics Journal, Dec. 2012

Book Chapters

L.Mountrichas, S.Siskos. Offset Reduction Techniques in Flash A/D Converters. In T.Noulis, M.Soma, Mixed-Signal Circuits. Taylor&Francis (to be published)

Conferences

L.Mountrichas, Th.Laopoulos, S.Siskos "A new 1.7GS/s 6-bit Flash A/D Converter", DCIS, Nov.2012

L.Mountrichas, Th.Laopoulos, S.Siskos "A 1.7GS/s 6-bit Flash A/D Converter with Distributed Offset Cancelling Sample-and-Hold", IEEE SOCC Sept. 2012

C.Vassou, **L.Mountrichas**, S.Siskos "A NMOS Bulk Voltage Trimming Offset Calibration Technique for a 6-bit 5GS/s Flash ADC", IEEE I2MTC May 2012

L.Mountrichas, S.Siskos "A novel switching scheme for offset storage cancellation technique, for GS/s range ADCs", IEEE I2MTC May 2012

P. Simitsakis, S. Liolis, D. Psyllos, **L. Mountrichas**, P. P. Sotiriadis **"**Design of a 1.2-V 60 GHz Transceiver in a 90nm CMOS RF Technology", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Beirut, Lebanon, Dec. 2011

EDUCATION

ARISTOTLE UNIVERSITY OF THESSALONIKI

Ph.D. Candidate in Electronics **2010-Present**

Electronics Lab, Department of Physics

Research Subject: "Design of integrated A/D and D/A Converters"

ARISTOTLE UNIVERSITY OF THESSALONIKI

M.Sc. Diploma in Electronic Physics (2 year course) – 8.78 / 10 **2007-2010**

Electronics Lab, Department of Physics

Thesis: "Design of a 90nm integrated comparator for a 6-bit, 2.5GHz flash A/D converter"

ARISTOTLE UNIVERSITY OF THESSALONIKI

B.Sc. Degree in Physics – 6.87 / 10 **2001-2007**

Areas of Concentration: Electronics and Telecommunications