Curriculum Vitae

Spyridon Nikolaidis

Last Name: Nikolaidis
First Name: Spyridon
Specialization: Analysis and design of digital circuits
Position: Associate Professor
Affiliation: Department of Physics, Aristotle University of Thessaloniki
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COURSES

Undergraduate courses

Digital Systems
Computer Architecture
Electronics: Laboratory course

Postgraduate courses

Digital Systems
Signals and Systems
Embedded Systems
Digital Systems Laboratory

RESEARCH INTERESTS

Delay modeling for logic CMOS gates
Power consumption modeling in logic gates and digital circuits
Low power design techniques for digital circuits and systems
High performance digital system design
Application Specific Instruction-set Processor (ASIP) design
Reconfigurable Instruction Set Processor (RISP) design
Power consumption modeling for processors

AWARDS

Best Conceptual Design Award for "*Designing a low-power soft-error fault-tolerant medicine infusion device*," in the context of DATE/Europractice design contest 2002, Paris 2002.

Best Award on Higher Education Program Student Design Contest 2002, SOC and PCB Category prizes for "*COSAFE: A low-power medicine infusion pump*," sponsored by Mentor Graphics & Sun Microsystems 2002.

Award of "Honorable mention for design contest entry" for "*AMDREL: A novel low-energy FPGA architecture and supporting CAD tool design flow*" International Conference on VLSI Design, Design Contest, Kolkata, India, Jenuary 2005.

4-th Position in the Design Contest of ASP-DAC 2005 (Asia South Pacific – Design Automation Conference) January 18-21, 2005, Shanghai, China for AMDREL: "Architectures and Methodologies for Dynamic REconfigurable Logic" IST-2001-34379, 5th IST Framework (1/3/2002–30/6/2005) http://vlsi.ee.duth.gr/amdrel.

Editor to ISRN Electronics http://www.isrn.com/journals/electronics/, 2011- today

Member of Organizing Committee in the conferences: ICECS 1999, PATMOS 1999, IFIP VLSI SoC 2008, PACET 2012.

Member of Technical Program Committee of the Design, Automation and Test in Europe Conference and Exhibition (DATE) for years 2007 and 2008 and for ICECS 2010.

Session chair in the conferences: ICECS 1999, ICECS 2001, PATMOS 2004, IDAACS 2005, ICECS 2010, PACET 2012.

Organization of a Special Session "Advances in Nanoscale Devices and Systems: Modeling, Design, Optimization" in the context of the IEEE Mediterranean Electrotechnical Conference (MELECON), Tunis, March 2012.

Organization of a Special Session "Advances in Nanoscale Devices and Systems: Modeling, Design, Testing" in the context of the IEEE International Conference on Electronics, Circuits and Systems (ICECS), Seville, Spain, 9-12 Dec. 2012.

Organization of the Workshop on Modern Circuits and Systems Technologies (MOCAST) at Thessaloniki, Greece, for the years 2012, 2013 and 2014.

Organization of a Summer School on "Power analysis, Modeling, Design and Optimization at Nanoscale technology" at Jordan University of Science and Technology (JUST) in Irbid, Jordan, 10-14 June, 2012. Invited instructors: prof. Kaushik Roy, Purdue, USA, prof. Bashir Hashimi, Southampton, UK, prof. Mohammed Ismail, Ohio State University, USA, prof. Ghassan O Shobaki, PUST, Jordan, prof. Jaan Raik, Tallinn, Estonia, prof. Rodrico Picos, UIB, Spain.

PROJECTS

European Projects

1. Scientific responsible for his University in the “Jordan Europe Wide Enhanced research Links in ICT”, Coordination and Support action, No 26650
2. Scientific responsible for his University in the “Energy Aware System-on-Chip Design of the HIPERLAND/2 standard” (EASY) IST-2000-30093.
3. Main researcher in the “Architectures and Methodologies for Dynamic Reconfigurable Logic” (AMDREL) IST-2001-34379.
4. Researcher in International Cooperation Program Greece-Ukraine with title “Instruction parameter analysis for power dissipation modeling in embedded microprocessors”.
5. Main researcher in the ”Low Power Hardware-Software Co-Design for Safety-Critical Applications” (COSAFE), ESPRIT 28593.
6. Researcher in the "Demonstrate OMI technology in computing clusters and storage systems – project 20290 DOMITIUS ESPRIT".
7. Researcher in the “Special action in microelectronics Hellenic VLSI Design and Prototyping Environment “ (HVLSI-DPE), Project 5692 ESPRIT.
8. Researcher in the “Cooperative Diagnosis and Therapy “ (TELEMED), RACE (R1086).

He has also participated in many national projects.

PUBLICATIONS

Sections in Books

1. “Designing CMOS Circuits for Low Power” Kluwer Academic Publishers, 2002.
   ISBN: 1-4020-7234-1.

Chapter 4: **S. Nikolaidis**, A. Chatzigeorgiou, “Circuit-Level Low-Power Design”pp.45-69.
Chapter 7: A. Chatzigeorgiou, **S. Nikolaidis**, “Reducing Power Consumption in Memories” pp. 117-140.
Editors: D. Soudris, C. Piguet, C.E. Goutis

2. “Fine- and Coarse-Grain Reconfigurable Computing” Spinger, 2007.
   ISBN: 978-1-4020-6504-0

Chapter 3: D. Soudris, K. Tatas, K. Siozios, G. Koutroumpezis, **S. Nikolaidis**, S. Siskos, N. Vasiliadis, V. Kalenteridis, H. Pournara, I. Pappas. « Amdrel. A Low Power FPGA Architecture and Supporting CAD Tool Design Flow” pp.153-180.
Editors: Stamatis Vassiliadis, Dimitrios Soudris

A. ***Publications in international Journals***

[A46] Stavros Stavrinides, Nikos Karagiorgos, Kostas Papathanasiou, **Spyridon Nikolaidis**, Antonios Anagnostopoulos,"A digital non – autonomous chaotic oscillator suitable for information transmission," IEEE Transactions on CAS II, Vol. 60, No 12, Dec. 2013.
[A45] C.L Sotiropoulou, L. Voudouris, Ch. Gentsos, A. Demiris, N. Vassiliadis, **S. Nikolaidis**, “Real-Time Machine Vision FPGA Implementation for Microfluidic Monitoring on Lab-on-Chips” IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), 2013, DOI: 10.1109/TBCAS.2013.2260338.
[A44] K. Papathanasiou, L. Voudouris, S. G. Stavrinides, **S. Nikolaidis**, “Applied Chaos: Linearizing Multibit ΔΣ Converters for Telecom Applications,” Journal of Concrete and Applicable Mathematics, Vol. 9, No 3, pp.197-204, 2011.
[A43] N. Kavvadias, **S. Nikolaidis**, “Scalable register bypassing for FPGA-based processors,” (2009) Microprocessors and Microsystems, 33 (7-8), pp. 441-452.

[A42] N. Vassiliadis, G. Theodoridis, and **S. Nikolaidis**, “An Application Development Framework for ARISE Reconfigurable Processors,” ACM Transactions on Reconfigurable Technology and Systems, Volume 2, Issue 4, No 24, pp. 24:1-24:30, Sept. 2009.

[A41] **S. Nikolaidis**, “Input Mapping Algorithm for Parallel Transistor Structures,” International Journal of Circuit Theory and Applications, John Wiley and Sons Ltd, Volume 37, Issue 7, pp. 856-861, Sept. 2009.

[A40] G. Theodoridis, N. Vasiliadis, **S. Nikolaidis**, “An ILP Model for Mapping Applications on Hybrid Systems,” IET Computers & Digital Techniques, Vol. 3, No. 1, pp. 33-42, 2009.

[A39] N. Vassiliadis, G. Theodoridis, and **S. Nikolaidis**, "The ARISE Approach for Extending Embedded Processors with Arbitrary Hardware Accelerators,” IEEE Transactions on Very Large Scale Integration Systems, Vol. 17, No 2, pp.221-233, Feb. 2009.

[A38] V. Konstadakos, A. Chatzigeorgiou, **S. Nikolaidis**, Th. Laopoulos, “Energy Consumption Estimation in Embedded Systems,” IEEE Transactions on Instrumentation and Measurement, Vol. 57, No 4, pp. 797-804, April 2008.

[A37] N. Kavvadias, **S. Nikolaidis**, “Elimination of overhead operations in complex loop structures for embedded microprocessors,” IEEE Transactions on Computers, Vol.57, No 2, pp. 200-214, Feb. 2008.

[A36] N. Vassiliadis, G. Theodoridis, and **S. Nikolaidis**, “Exploring Opportunities to Improve the Performance of a Reconfigurable Instruction Set Processor,” International Journal of Electronics, Vol. 94, No. 5, pp. 481-500, May 2007.

[A35] N. Kavvadias, V. Giannakopoulou, **S. Nikolaidis**, “Development of a customized processor architecture for accelerating genetic algorithms,” Journal of Microprocessors and Microsystems, 31, 347-359, 2007

[A34] **S. Nikolaidis,** Th. Nikolaidis, “Analyzing the Operation of the Basic Pass Transistor Structure,” International Journal of Circuit Theory and Applications, Wiley publications, Jan/Feb 2007, 35, pp.1-15.

[A33] V. Konstantakos, K. Kosmatopoulos, **S. Nikolaidis**, Th. Laopoulos, “Measurement of Power Consumption in Digital Systems,” IEEE Transactions on Instrumentation and Measurement, Vol. 55, No. 5, pp. 1662-1670, Oct. 2006.

[A32] L. Bisdounis, S. Blionas, E. Macii, **S. Nikolaidis**, R. Zafalon, “Implementation Strategy and Results of an Energy-Aware System-on-Chip for 5 GHz WLAN Applications,” Journal of Low-Power Electronics, Vol 2, pp. 18-26, 2006.

[A31] N. Vassiliadis, N. Kavvadias, G. Theodoridis, and **S. Nikolaidis**, “A RISC architecture extended by an efficient tightly coupled reconfigurable unit,” International Journal of Electronics, vol. 93, no 6, pp.421-438, June 2006.

[A30] Vassiliadis N., Chormoviti A., Kavvadias N., **Nikolaidis S**., “The Effect of Data-Reuse Transformations on Multimedia Applications for Application Specific Processors,’ International Scientific Journal of Computing, Vol.4, Issue 3, pp. 102-109, 2005.

[A29] K. Siozios, G. Koutroumpezis, K. Tatas, N. Vassiliadis, V. Kalenteridis, H. Pournara, I. Pappas, D. Soudris, **S. Nikolaidis**, S. Siskos, “A Novel FPGA Architecture and an Integrated Framework of CAD Tools for Implementing Applications,” IEICE Transactions on Information and Systems, vol. E85-A/B/C/D, No 1, pp.1369-1380, March 2005.

[A28] **S. Nikolaidis**, A. Chatzigeorgiou, T. Laopoulos, “Developing an Environment for Embedded Software Energy Estimation,” Journal on Computer Standards & Interfaces, 28, pp. 150-158, 2005.

[A27] N. Kavvadias, **S. Nikolaidis**, “Zero-overhead loop controller for implementing multimedia algorithms,” IEE Proceedings Computers & Digital Techniques, Vol. 152, No. 4, pp. 517-526, July 2005.

[A26] V. Kalenteridis, H. Pournara, K. Siozos, K. Tatas, G. Koutroumpezis, N. Vassiliadis, I.Pappas, **S. Nikolaidis**, S.Siskos, D. J. Soudris and A. Thanailakis, “A Complete Platform

and Toolset for System Implementation on Fine-Grain Reconfigurable Hardware," Journal on Microprocessors and Microsystems, Vol 29/6, pp 247-259, 2005.

[A25] **S. Nikolaidis**, N. Kavvadias, T. Laopoulos, L. Bisdounis and S. Blionas, "Instruction Level Energy Modeling for Pipelined Processors," Journal of Embedded Computing, IOS press, Issue 3, Vol.1, pp. 317-324, 2005.

[A24] N. Kavvadias, P. Neofotistos, **S. Nikolaidis,** K. Kosmatopoulos, T. Laopoulos, "Measurements Analysis of the Software-Related Power Consumption of Microprocessors," IEEE Transactions on Instrumentation and Measurement, vol. 53, no 4, pp.1106-1112, August 2004.

[A23] S. Kougia, A. Chatzigeorgiou, **S. Nikolaidis**, "Evaluating Power Efficient Data-Reuse Decisions for Embedded Multimedia Applications: An Analytical Approach," Journal of Circuits, Systems and Computers, Vol. 13, No. 1, pp. 151-180, February 2004.

[A22] T. Laopoulos, P. Neofotistos, K. Kosmatopoulos, **S. Nikolaidis**, "Measurement of Current Variations for the Estimation of Software-related Power Consumption," IEEE Transactions on Instrumentation and Measurement, Vol 52, No 4, pp. 1206-1212, August 2003.

[A21] **S. Nikolaidis**, E. Karaolis, A. Kakarountas, K. Papadomanolakis, C.E. Goutis, "A Methodology for Calculating the Undetectable Double-Faults in Self Checking Circuits," Journal of Circuits, Systems and Computers, Vol. 12, No. 1, pp.75-91, Feb. 2003.

[A20] A. Chatzigeorgiou, **S. Nikolaidis,** "Efficient Output Waveform Evaluation of a CMOS Inverter based on Short-Circuit Current Prediction," International Journal of Circuit Theory and Applications, vol 30, Issue 5, pp.547-566, Sept/Oct. 2002.

[A19] E.D. Kyriakis-Bitzaros, **S. Nikolaidis**, "Estimation of Bit-Level Transition Activity in Data-Paths Based on Word-Level Statistics and Conditional Entropy," IEE Proceedings on Circuits, Devices and Systems, vol 149, Issue 4, pp. 234-240, Aug. 2002.

[A18] **S. Nikolaidis**, T. Laopoulos, "Instruction-level power consumption estimation of embedded processors for low-power applications," Journal on Computer Standards & Interfaces, Vol. 24, No. 2, pp. 133-137, 2002.

[A17] A. Chatzigeorgiou and **S. Nikolaidis**, "Modeling the Operation of Pass Transistor and CPL Gates," International Journal of Electronics, Vol. 88, No. 9, pp.977-1000, May 2001.

[A16] A. Chatzigeorgiou, **S. Nikolaidis**, I. Tsoukalas, "Modeling CMOS Gates Driving RC Interconnect Loads," IEEE Transanctions on Circuits and Systems II, Vol. 48, No.4, pp. 413-418, Apr. 2001.

[A15] A. Chatzigeorgiou and **S. Nikolaidis**, "Single Transistor Primitive For Timing and Power Modeling of CMOS Gates," International Journal of Electronics, Vol. 87, No. 10, pp. 1227-1238, 2000.

[A14] **S. Nikolaidis**, E. Karaolis, E.D. Kyriakis-Bitzaros, "Estimation of Signal Transition Activity in FIR Filters Implemented by MAC Architecture," IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 19, No. 1, pp.164-169, Jan. 2000.

[A13] **S. Nikolaidis**, E.D. Kyriakis-Bitzaros, "A Charge Recycling Technique for the Design of Low Power CMOS Clock Drivers," Journal of Circuits, Systems and Computers, Vol. 9, Nos. 3 & 4, pp.169-180, 1999.

[A12] L. Bisdounis, O. Koufopavlou, **S. Nikolaidis**, "Modeling Output Waveform and Propagation Delay of a CMOS Inverter in the Submicron Range," IEE Proceedings on Circuits, Devices and Systems, Vol. 145, Issue 6, pp. 402-408, Dec. 1998.

[A11] A. Chatzigeorgiou, **S. Nikolaidis**, I. Tsoukalas, "Estimating starting point of conduction of CMOS gates," Electronics Letters of IEE, pp. 1622-1624, Vol. 34, No 17, Aug. 1998.

[A10] A. Chatzigeorgiou, **S. Nikolaidis**, "Input Mapping Algorithm for Modelling of CMOS Circuits," Electronics Letters of IEE, pp. 1177-1179, Vol 34, No 12, June 1998.

[A9] A. Chatzigeorgiou, **S. Nikolaidis**, “Collapsing the CMOS Transistor Chain to An Effective Single Equivalent Transistor,” IEE Proceedings on Circuits, Devices and Systems, Vol.145, No 5, pp.347-353, Oct. 1998.

[A8] L. Bisdounis, **S. Nikolaidis**, O. Koufopavlou, “Analytical model for the CMOS Short-Circuit Power Dissipation,” Integrated Computer-Aided Engineering, IOS Press, Vol.5, No 2, pp.129-140, Apr.1998.

[A7] **S. Nikolaidis**, A. Chatzigeorgiou, “Analytical Estimation of Propagation Delay and Short-Circuit Power Dissipation in CMOS Gates,” International Journal of Circuit Theory and Applications, Wiley publications, Vol. 27, pp.375-392, 1999.

[A6] A. Chatzigeorgiou, **S. Nikolaidis**, I. Tsoukalas, “A Modeling Technique for CMOS Gates,” IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 18, No 5, pp.557-575, May 1999.

[A5] **S. Nikolaidis**, A. Chatzigeorgiou, “Modeling the Transistor Chain Operation in CMOS Gates for Short Channel Devices,” IEEE Transactions on Circuits and Systems-I, Vol. 46, No 10, pp. 1191-1202, Oct. 1999.

[A4] L. Bisdounis, **S. Nikolaidis**, O. Koufopavlou, “Analytical Transient Response and Propagation Delay Evaluation of the CMOS Inverter for Short-channel Devices,” IEEE Journal of Solid-State Circuits, Vol. 33, No 2, pp. 302-306, Feb. 1998.

[A3] L. Bisdounis, **S. Nikolaidis**, O. Koufopavlou, “Propagation Delay and Short-Circuit Power Dissipation Modeling of the CMOS Inverter,” IEEE Transanctions on Circuits and Systems I, Vol.45, No 3, pp.259-270, Mar 1998.

[A2] **S.S. Nikolaidis**, S. Theodoridis, C.E Goutis, “Array Processor for Block Adaptive LS FIR Filtering,” Signal Processing, Elsevier, Vol.39, pp. 215-222, 1994.

[A1] **S.S Nikolaidis**, J.N. Mourjopoulos, C.E. Goutis, “A Dedicated Processor for Time-Varying Digital Filters,” IEEE Transanctions on Circuits and Systems, Vol. CAS-40, No 7, pp. 452-455, Jul.1993.

B. *Publications in international Journals* as Conference Proceedings

[B5] I. Pappas, V. Kalenteridis, N. Vassiliadis, H. Pournara, K. Siozios, G. Koutroumpezis, K. Tatas, **S. Nikolaidis**, S. Siskos, D. Soudris, A. Thalainakis, "Fine-grain reconfigurable platform: FPGA hardware design and software toolset development," Journal of Physics: Conference Series,Vol. 10, Issue 1, pages 252-256, 1 Jan. 2005.

[B4] G.P. Economou, **S.S. Nikolaidis**, D.E. Metafas, C.E. Goutis, “Development of a Technology Independent Library,” Journal of Microprocessing and Microprogramming 39, 1993, pp. 241-244.

[B3] D.E Metafas, E.Mariatos, **S.S.Nikolaidis**, C.E. Goutis, “Implementation of Given’s Rotation Processors for DSP Real-Time Applications,” Journal of Microprocessing and Microprogramming 38, 1993, pp. 351-357.

[B2] D.E Metafas, **S.S. Nikolaidis**, C.E. Goutis, “Real Time Cepstrum Computation Based on an Advanced CORDIC Processor,” Journal of Microprocessing and Microprogramming 37, 1993, pp. 57-60.

[B1] **S.S Nikolaidis**, O.G. Koufopavlou, S. Theodoridis, C.E. Goutis, “Array Processor for LS FIR System Identification,” Journal of Microprocessing and Microprogramming 32, Aug.1991, pp. 557-563.

C. *Presentations in Conferences and Workshops*

[C96] D. Tassis, I. Messaris, N. Fasarakis, **S. Nikolaidis**, G. Ghibaudo and C. Dimitriadis, " Variability Analysis – Prediction Method for Nanoscale Triple Tate FinFETs," 29th International Confernce on Mictoelectronics (MIEL), Belgrade, Serbia, 12-15 May, 2014.

[C95] C.-L. Sotiropoulou, Ch. Gentsos, **S. Nikolaidis**, "High Performance Median FPGA Implementation for Machine Vision Applications," International Conference on Electronics, Circuits and Systems (ICECS), Abu Dhabi, Dec 8-11, 2013.

[C94] O. Palampougioukis, **S. Nikolaidis**, "An efficient model of the CMOS inverter for nanometer technologies," International Conference on Electronics, Circuits and Systems (ICECS), Abu Dhabi, Dec 8-11, 2013.

[C93] G. Volpi, C.-L. Sotiropoulou, **S. Nikolaidis** et al. "Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger," to be published in the Proceedings of TWEPP 2013, Perugia, Italy (abstact submission)

[C92] C.-L. Sotiropoulou, A. Annovi, M. Beretta, P. Luciano, P. Giannetti and S. Nikolaidis, "A Multi-Core FPGA-based 2D-Clustering Algorithm for High- Throughput Data Intensive Applications," 14th ICATPP Conference on Astroparticle, Particle, Space Physics and Detectors for Physics Applications, Como, Italy, 23-27 September 2013. (abstact submission)

[C91] C.-L. Sotiropoulou, A. Annovi, M. Beretta, P. Luciano and S. Nikolaidis, "A Multi-Core FPGA-based Clustering Algorithm for Real-Time Image Processing," to be published in the proceedings of IEEE-NSS 2013, COEX, Seoul, Korea(abstact submission)

[C90] Panagiotis Chaourani, **Spyridon Nikolaidis**, Abdoul Rjoub, "Subthreshold influence on Pass Transistor Operation Modeling for Nano-Scale Technologies," The 8th Jordanian International Electrical & Electronics Engineering Conference, Amman, 16-18 April 2013.

[C89] Dimitrios Tzagkas, **Spyridon Nikolaidis**, Abdoul Rjoub "Estimating the Starting Point of Conduction in Nanoscale CMOS Gates," International Conference on Electronics, Circuits and Systems (ICECS), Seville, Spain, pp. 957-960, 9-12 Dec. 2012.

[C88] L. Voudouris, C.L. Sotiropoulou, N. Vasiliadis, A. Demiris, S. Nikolaidis, " High-speed FPGA-based Flow Detection for Microfluidic Lab-on-Chip," 20th Mediterranean Conference on Control & Automation (MED), Barcelona, Spain, pp. 1434-1439, July 3-6, 2012.

[C87] C-L. Sotiropoulou, L. Voudouris, C. Gentsos, N. Vasiliadis, A. Demiris, **S. Nikolaidis**, S. Blionas, "FPGA-Based Machine Vision Implementation for Lab-on-Chip Flow Detection", IEEE International Symposium on Circuits & Systems, Seoul, Korea, pp. 2047-2050, May 20-23, 2012.

[C86] I. Pappas, L. Voudouris, **S. Nikolaidis**, A. Rjoub, "A new current – programmed pixel design for AMOLED displays implemented with organic thin film transistors," International Conference on Microelectronics, MIEL 2012 Conference, Nis, Serbia, May 13-16, pp. 77-80, 2012.

[C85] L. Voudouris, A. Rjoub, **S. Nikolaidis,** "High speed FPGA implementation of Hough transform for real-time applications", IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Tallinn, Esthonia, April 18-20, pp. 213-218, 2012.

[C84] D Tzagkas, C. Varnavidou, I. Pappas, L. Voudouris, A. Rjoub, **S. Nikolaidis**, "Pass transistor driving RC loads in nanoscale technologies," IEEE Mediterranean Electrotechnical Conference (MELECON), Tunisia, March 26-28, pp. 76-79, 2012.

[C83] Calliope-Louisa Sotiropoulou**, Spiridon Nikolaidis,** "ILP Formulation for Hybrid FPGA MPSoCs Optimizing Performance, Area and Memory Usage," International Conference on Electronics, Circuits and Systems (ICECS), Beirut, Lebanon, pp. 748-751, Dec. 2011.

[C82] Calliope-Louisa Sotiropoulou, Christos Gentsos, **Spiridon Nikolaidis** and Abdoul Rjoub, "FPGA-based Canny Edge Detection for Real-Time Applications," 26th Conference on

Design of Circuits and Integrated Systems (DCIS), Albufeira, Portugal, pp. 73-77, Nov. 2011

[C81] P. Chaourani, I. Pappas, **S. Nikolaidis**, A. Rjoub, "Pass transistor operation for rising ramps in both terminal inputs," 26th Conference on Design of Circuits and Integrated Systems (DCIS), Portugal, pp. 475-480, Nov. 2011

[C80] P. Chaourani, I. Pappas, **S. Nikolaidis**, A. Rjoub, "Pass transistor operation modeling for nanoscale technologies,"International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 53-62, Madrid, Spain, Sept. 2011.

[C79] Christos Gentsos, Calliope-Louisa Sotiropoulou**,** Nikolaos Vassiliadis, **Spiridon Nikolaidis,** "Real Time Canny Edge Detection Parallel Implementation for FPGAs" International Conference on Electronics, Circuits and Systems (ICECS), Athens, Greece, , pp. 499-502, Dec. 2010.

[C78] Calliope-Louisa Sotiropoulou**, Spiridon Nikolaidis,** "Design Space Exploration for FPGA-based Multiprocessing Systems" International Conference on Electronics, Circuits and Systems (ICECS), Athens, Greece, pp. 1164-1167, Dec. 2010.

[C77] K. Papathanasiou, L. Voudouris, S.G. Stavrinides, **S. Nikolaidis**, "Applied Chaos: Linearizing Multibit ΔΣ Converters for Telecom Applications," 3rd International Interdisciplinary Chaos Symposium on "Chaos and Complex Systems", CCS2010, Instabul, Turkey, May 2010.

[C76] N. Vassiliadis, G. Theodoridis, **S. Nikolaidis,** "A Flexible Simulation Framework for Reconfigurable Processors," 16th IFIP/IEEE International Conference on Very Large Scale Integration, Rhodes Island, Greece, pp. 140-143, Oct. 2008.

[C75] N. Kavvadias, **S. Nikolaidis,** "The ByoRISC configurable processor family," 16th IFIP/IEEE International Conference on Very Large Scale Integration, Rhodes Island, Greece, pp. 439-444, Oct. 2008.

[C74] N. Vassiliadis, G. Theodoridis, **S. Nikolaidis**, "ARISE Machines: Extending Processors with Hybrid Accelerators," International Workshop on Applied Reconfigurable Computing (ARC), London, UK, pp. 196-208, March, 2008.

[C73] N. Vassiliadis, G. Theodoridis, S. Nikolaidis, "The ARISE Reconfigurable Instruction Set Extensions Framework," International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS), Samos, Greece, pp. 153-160, Jule 2007.

[C72] N. Kavvadias, S. Nikolaidis, 'YARDstick: Automation tool for custom processor development," U-Booth presedation in DATE Conference, Nice, France, April 2007.

[C71] N. Kavvadias, S. Nikolaidis**, "**A Flexible Instruction Generation Framework for Extending Embedded Processors," 13th IEEE Mediterranean Electrotechnical Conference (MELECON), Malaga, Spain, pp. 125-128, May 2006.

[C70] V. Konstantakos, A. Chatzigeorgiou, **S. Nikolaidis,** T. Laopoulos, "Energy consumption estimation in embedded systems," IEEE Instrumentation and Measurement Technology Conference (IMTC), Sorrento, Italy, April 24-27, pp. 235-238, 2006.

[C69] N. Vassiliadis, G. Theodoridis, **S. Nikolaidis**, " An Automated Development Framework for a RISC Processor with Reconfigurable Instruction Set Extensions," in IPDS 2006: 20th International Parallel and Distributed Processing Symposium, Rhodes Island, Greece, April 2006.

[C68] N. Vassiliadis, G. Theodoridis, **S. Nikolaidis,** "Enhancing a Reconfigurable Instruction Set Processor with Partial Predication and Virtual Opcode Support," International Workshop on Applied Reconfigurable Computing (ARC), Delft, The Netherlands, 1-3 March, 2006

[C67] N. Kavvadias**, S. Nikolaidis,** "A portable specification of zero-overhead looping control hardware applied to embedded processors," IEEE International Symposium on Circuits and Systems (ISCAS), Kos, Greece, May 21-24, pp. 1599-1602, 2006.

[C66] L. Bisdounis, S. Blionas, E. Macii, **S. Nikolaidis**, R. Zafalon, «Energy-aware system-on-chip for 5 GHz wireless LANs,» International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS'05), pp. 166-176, Leuven, Belgium, Sept 2005.

[C65] V. Konstantakos, K. Kosmatopoulos, **S. Nikolaidis**, Th. Laopoulos, "In-Chip Configuration for Monitoring Power Consumption in Micro-processing Systems," IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS'2005), pp. 156-161, Sofia, Bulgaria, Sep. 2005.

[C64] A. Chormoviti, N. Vassiliadis, G. Theodoridis, **S. Nikolaidis**, "Enhancing Embedded Processors with Specific Instruction Set Extensions for Network Applications," IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS'2005), pp. 199-203, Sofia, Bulgaria, Sep., 2005.

[C63] Vassiliadis N., Chormoviti A., Kavvadias N., **Nikolaidis S**., "The Effect of Data-Reuse Transformations on Multimedia Applications for Application Specific Processors," IEEE International Workshop on Intelligent Data Acquisition and Advanced Computing Systems: Technology and Applications (IDAACS'2005), pp. 179-182, Sofia, Bulgaria, Sep., 2005.

[C62] K. Zotos, A. Litke, A. Chatzigeorgiou, **S. Nikolaidis**, G. Stephanides, "Energy Complexity of Software in Embedded Systems," IASTED International Conference on Software Engineering (ACIT-SE 2005), Novosibirsk, Russia, June 20-24, 2005.

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