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About me

I received my Diploma, Master and Ph.D Degree in Electrical and Computer Engineering from the Democritus University of Thrace, Greece, in 2001, 2003 and 2009, respectively. From 2009-2016, I was senior research associate in the National Technical University of Athens (N.T.U.A.), Greece. Currently I am working as assistant professor at school of Physics at Aristotle University of Thessaloniki (A.U.TH.). Starting from 2002 I have worked as principal investigator in numerous research projects funded from the European Commission (E.C.), European Space Agency (E.S.A.), as well as the Greek Government and Industry.

Research Topics

- Heterogeneous FPGAs
- CAD Algorithms
- 3-D Integration
- Fault Tolerance
- Virtualization
- Network-on-Chip

I. Σπουδές

2003–2009 Διδακτορικό Δίπλωμα Ηλεκτρολόγου Μηχανικού και Μηχανικού Η/Υ.
Τμήμα Ηλεκτρολόγων Μηχανικών & Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης (Δ.Π.Θ.).
Τίτλος Διατριβής: "*Σχεδιασμός Υλικού και Λογισμικού Επαναδιαμορφούμενων Συστημάτων VLSI με Χαμηλή Κατανάλωση Ισχύος*".

2001–2003 Μεταπτυχιακό Δίπλωμα Ειδίκευσης Ηλεκτρολόγου Μηχανικού και Μηχανικού Η/Υ.
Τμήμα Ηλεκτρολόγων Μηχανικών & Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης (Δ.Π.Θ.).
Τίτλος Διατριβής: "*Σχεδιασμός Βασικής Δομικής Μονάδας και Ανάπτυξη Εργαλείων Σχεδιασμού για Ενσωματωμένο FPGA*".

1996–2001 Δίπλωμα Ηλεκτρολόγου Μηχανικού και Μηχανικού Η/Υ.
Τμήμα Ηλεκτρολόγων Μηχανικών & Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης (Δ.Π.Θ.).

II. Ερευνητικές Δραστηριότητες

- Σχεδιασμός υλικού και εργαλείων λογισμικού για επαναδιαμορφούμενες αρχιτεκτονικές.
- Σχεδίαση αρχιτεκτονικών και εργαλείων λογισμικού για αυξημένη αξιοπιστία σε κυκλώματα VLSI.
- Ανάπτυξη CAD αλγορίθμων και εργαλείων VLSI.
- Σχεδιασμός υλικού και λογισμικού ενσωματωμένων συστημάτων.
- Σχεδιασμός τρισδιάστατων (3Δ) αρχιτεκτονικών.
- Ανάπτυξη μεθοδολογιών και εργαλείων για έξυπνες πόλεις (smart cities).
- Τεχνολογίες για CyberPhysical Systems (CPS).
- Τεχνολογίες για Internet-of-Things (IoT).
- Ανάπτυξη/Μοντελοποίηση δικτύων σε ψηφίδα (Network-On-Chip).
- Εικονική προτυποποίηση.

III. Συμμετοχή σε Ερευνητικά & Αναπτυξιακά Προγράμματα

Α. Χρηματοδοτούμενα από την Ευρωπαϊκή Ένωση

1. AMDREL: Architectures and Methodologies for Dynamic REconfigurable Logic (IST-2001-34379).
2. MORPHEUS: Multi-purpose Dynamically Reconfigurable Platform for intensive Heterogeneous processing, 2005-IST-027342, 6th Framework, 2nd Phase.
3. MOSART: Mapping Optimization for Scalable multi-core ARchiTecture, 7th IST Framework, STREP.
4. MNEMEE: Memory management technology for adaptive and efficient design of embedded systems, 7th IST Framework, No. 216224, STREP.
5. 2PARMA: PARallel Paradigms and Run-time Management techniques for Many-core Architectures
6. INERTIA: Integrating Active, Flexible and Responsive Tertiary Prosumers into a Smart Distribution
7. NOPTILUS, Framework Programme ICT-FP7
8. FABSPACE 2.0: The Fablab for geodata-driven innovation - by leveraging Space data in particular, in Universities 2.0

Β. Χρηματοδοτούμενα από την Ευρωπαϊκή Υπηρεσία Διαστήματος (ESA)

1. SPARTAN: Sparing Robotics Technologies for Autonomous Navigation
2. SEXTANT: Sparing Robotics Technologies for Autonomous Navigation

Γ. Λοιπά Έργα Χρηματοδοτούμενα από Ευρωπαϊκούς Οργανισμούς

1. HIPEAC (European Network of Excellence on High-Performance Embedded Architecture and Compilation): "On Providing Dynamic Reliability Improvement in FPGAs
2. TEACHER: TEach AdvanCEd Reconfigurable architectures and tools (Funded by DAAD).

Δ. Εθνικά Έργα

1. ΔΙΑΣ: Ανάπτυξη συστήματος βασικής ζώνης για ΔΙαμόρφωση και Αποδιαμόρφωση Σήματος (baseband modem) σε ευρυζωνικά ασύρματα δίκτυα εξωτερικών χώρων (outdoor broadband wireless networks)
2. ΠΕΝΕΔ'03: Σχεδιασμός ενσωματωμένων συστημάτων με χαμηλή κατανάλωση ενέργειας για την υλοποίηση εφαρμογών πολυμέσων και ασύρματων δικτύων (Design of Low Power Embedded Systems for Implementation of Multimedia and Wireless LAN Networks)
3. Πυθαγόρας ΙΙ – Μεθοδολογία Σχεδιασμού Ενσωματωμένων Συστημάτων Χαμηλής Κατανάλωσης Ισχύος για Υλοποίηση Εφαρμογών Πολυμέσων και Ασυρμάτων Δικτύων.
4. NexGenMiliWave: Μικροκυματική Ραδιοζεύξη Επόμενης Γενιάς – ΜΙΚΡΟ2-ΣΕ-Β/Ε-ΙΙ
5. MENELAOS: Hellenic Space Technologies and Applications Cluster (si-Cluster)
6. CIDCIP: Hellenic Space Technologies and Applications Cluster (si-Cluster)

IV. ΚΑΤΑΛΟΓΟΣ ΕΠΙΣΤΗΜΟΝΙΚΩΝ ΕΡΓΑΣΙΩΝ

Α. Διδακτορική Διατριβή

Α1. Κωνσταντίνος Σιώζιος, "*Σχεδιασμός Υλικού και Λογισμικού Επαναδιαμορφούμενων Συστημάτων VLSI με Χαμηλή Κατανάλωση Ισχύος*", Τμήμα Ηλεκτρολόγων Μηχανικών και Μηχανικών Υπολογιστών, Δημοκρίτειο Πανεπιστήμιο Θράκης.

Β. Βιβλία

Β1. "*Designing 2D and 3D Network-on-Chip Architectures*", Editors: K. Tatas, K. Siozios, A. Jantsch and D. Soudris, Springer, 2014.

Β2. K. Siozios, D. Soudris and E. Kosmatopoulos "*CyberPhysical Systems: Decision Making Mechanisms and Applications*", River Publishers (available mid of 2017).

Γ. Κεφάλαια σε Βιβλία

Γ1. D. Soudris, K. Tatas, K. Siozios, G. Koutroumpezis, S. Nikolaidis, S. Siskos, N. Vassiliadis, V. Kalenteridis, H. Pournara and I. Pappas, "*AMDREL: A Novel Low-Energy FPGA Architecture and Supporting CAD Tool Design Flow*", Book Chapter in "*Fine- and Coarse-Grain Reconfigurable Systems*", Editors: S. Vassiliadis and D. Soudris, pp. 152–180, Springer, 2007.

Γ2. K. Tatas, K. Siozios, and D. Soudris, "*A Survey of Existing Fine-Grain Reconfigurable Architectures and CAD Tools*", Book Chapter in "*Fine- and Coarse-Grain Reconfigurable Systems*", Editors: S. Vassiliadis and D. Soudris, pp. 3–88, Springer, 2007.

Γ3. A. Bartzas, K. Siozios, and D. Soudris, "*Three Dimensional Network-on-Chip Architectures*", Book Chapter "*Networks on Chips: Theory and practice*", Editors: F. Gebali, H. Elmiligi, M. W. El-Kharashi, pp. 1–28, CRC Press, 2008.

Γ4. K. Siozios and D. Soudris, "*A Temperature-Aware Placement and Routing Algorithm Targeting 3D FPGAs*", Book Chapter in "*VLSI-SOC: Design Methodologies for SoC and SiP*", pp. 211–231, Springer, Dordrecht/London/Boston, 2010.

Γ5. K. Siozios, H. Sidiropoulos and D. Soudris, "*Architectures and CAD Tools for 3D FPGAs*", Book Chapter in "*Reconfigurable Logic: Architecture, Tools and Applications*", pp. 489–511, CRC press, Oct. 2015.

Γ6. K. Siozios, P. Danassis, N. Zompakis, E. Kosmatopoulos and D. Soudris, "*Supporting Decision Making for Large-Scale IoTs: Trading Accuracy with Computational Complexity*", Book Chapter in "Components and Services for IoT Platforms: Paving the Way for IoT Standards", Editors: G. Keramidas, N. Voros and M. Hübner, pp. 233–250, Springer International Publishing, 2017.

Δ. Επιστημονικά Περιοδικά

Δ1. K. Siozios, G. Koutroumpezis, K. Tatas, N. Vassiliadis, V. Kalenteridis, H. Pournara, I. Pappas, D. Soudris, A. Thanailakis, S. Nikolaidis and S. Siskos, "*A Novel FPGA Architecture and an Integrated Framework of CAD Tools for Implementing Applications*", IEICE Transactions on Information and Systems, Vol. E88-D, No. 7, pp. 1369–1380, July 2005.

Δ2. V. Kalenteridis, H. Pournara, K. Siozios, K. Tatas, I. Pappas, S. Nikolaidis, S. Siskos, D. J. Soudris and A. Thanailakis, "*A Complete Platform and Toolset for System Implementation on Fine-Grain Reconfigurable Hardware*", Microprocessors and Microsystems, Elsevier Publishers, Vol. 29, Issue 6, pp. 247–259, August, 2005.

Δ3. K. Siozios, D. Soudris and A. Thanailakis, "*Designing a General-Purpose Interconnection Architecture for FPGAs*", Journal of Low-Power Electronics (JOLPE), Vol. 4 No. 1, pp. 34–47, April 2008.

Δ4. K. Siozios, D. Soudris and A. Thanailakis, "*A Software-Supported Methodology for Designing General-Purpose Interconnectior Networks for Reconfigurable Architectures*", International Journal of Computer Systems Science and Engineering (IJCSSE), Vol. 4, No. 3, pp. 187–199, Summer 2008.

Δ5. K. Siozios, D. Soudris, and A. Thanailakis, "*A Novel Allocation Methodology for Partial and Dynamic Bitstream Generation of FPGA Architectures*", Journal of Circuits, Systems, and Computers (JCSC), Vol. 19, No. 3, pp. 701–717, May 2010.

Δ6. K. Siozios, A. Bartzas and D. Soudris, "*Architecture-Level Exploration of Alternative Interconnection Schemes Targeting to 3D FPGAs: A Software-Supported Methodology*", International Journal of Reconfigurable Computing, Volume 2008 (2008), Article ID 764942, 18 pages, doi:10.1155/2008/764942.

Δ7. K. Siozios and D. Soudris, "*A Power-Aware Placement and Routing Algorithm Targeting 3D FPGAs*", Journal of Low Power Electronics (JOLPE), Vol. 4, No. 3, pp. 275–289, December 2008.

Δ8. K. Siozios and D. Soudris, "*Designing a Novel High-Performance FPGA Architecture for Data Intensive Applications*", Journal of Real-Time Image Processing, Springer Berlin/Heidelberg, Vol. 4, No. 2, pp. 155–166, June, 2009.

Δ9. K. Siozios and D. Soudris, "*A Methodology for Alleviating the Performance Degradation of TMR Solutions*", IEEE Embedded Systems Letters, Vol. 2, No. 4, pp. 111–114, Dec. 2010.

Δ10. K. Siozios, V.F. Pavlidis, and D. Soudris, "*A Novel Framework for Exploring 3-D FPGAs with Heterogeneous Interconnect Fabric*", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 5, No. 1, pp. 4:1–4:23, March 2012.

Δ11. K. Siozios and D. Soudris, "*A Tabu-based Partitioning and Layer Assignment Algorithm for 3-D FPGAs*", IEEE Embedded Systems Letters, Vol. 3, No. 3, pp. 97–100, September 2011.

Δ12. K. Siozios, D. Rodopoulos and D. Soudris, "*On Supporting Rapid Thermal Analysis*", IEEE Computer Architecture Letters, Vol. 10, No. 2, pp. 53–56, July-December, 2011.

Δ13. H. Sidiropoulos, K. Siozios and D. Soudris, "*On Supporting Rapid Exploration of Memory Hierarchies onto FPGAs*", Journal of Systems Architecture, Vol. 59, No. 2, pp. 78–90, Feb. 2013 (invited from paper E37).

Δ14. D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, "*A Systematic Methodology for Reliability Improvements on SoC-based Software Defined Radio Systems*", VLSI Design, Vol. 2012, Article ID 784945, 15 pages.

Δ15. D. Diamantopoulos, K. Siozios and D. Soudris, "*A Framework for Performing Rapid Evaluation of 3-D SoCs*", IET Electronics Letters, pp. 679–681, June 2012.

Δ16. K. Tatas, K. Siozios, A. Bartzas, C. Kyriacou and D. Soudris, "*A Novel Prototyping and Evaluation Framework for NoC-based MPSoC*", International Journal of Adaptive, Resilient and Autonomic Systems (IJARAS), Vol. 4, No. 3, pp. 1–24, 2013.

Δ17. H. Sidiropoulos, K. Siozios, P. Figuli, D. Soudris, M. Hubner and J. Becker, "*JITPR: A Framework for Supporting Fast Application's Implementation onto FPGAs*", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 6, No. 2, pp. 1–12, July 2013 (invited from paper E52).

Δ18. I. Kotsavelis, L. Nalpantidis, E. Boukas, M. Rodrigalvarez, I. Stamoulias, G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris and A. Gasteratos, "*SPARTAN: Developing a Vision System for Future Autonomous Space Exploration Robots*", Journal of Field Robotics, pp. 1–34, 2013.

Δ19. E. Sotiriou-Xanthopoulos, D. Diamantopoulos, K. Siozios, G. Economakos and D. Soudris, "*A Framework for Rapid Evaluation of Heterogeneous 3-D NoC Architectures*", Microprocessors and Microsystems, Vol. 38, pp. 292–303, 2014.

Δ20. K. Siozios and D. Soudris, "*A low-cost fault tolerant solution targeting commercial FPGA devices*", Journal of System Architecture (JSA), Vol. 59, pp. 1255-1265, 2013.

Δ21. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Novel 3-D FPGA Architecture Targeting Communication Intensive Applications*", Journal of Systems Architecture (JSA), Vol. 60, No. 1, pp. 32–39, Jan. 2014 (invited from paper E51).

Δ22. D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, "*GENESIS: Parallel Application Placement onto Reconfigurable Architectures*", ACM Transactions on Embedded Computing Systems, Vol. 14, No. 1, Article 18, 26 pages, January 2015 (invited from paper E61).

Δ23. K. Siozios, D. Soudris and M. Hubner, "*A Framework for Supporting Adaptive Fault Tolerant Solutions*", ACM Transactions on Embedded Computing Systems, Vol. 13, No. 5s, Article 169, pp. 1–25, Nov. 2014 (invited from paper E63).

Δ24. D. Diamantopoulos, E. Sotiriou-Xanthopoulos, K. Siozios, G. Economakos and D. Soudris, "*Plug&Chip: A Framework for Supporting Rapid Prototyping of 3-D Hybrid Virtual SoCs*", ACM Transactions on Embedded Computing Systems, Vol. 13, No. 5s, Article 168, pp. 1–25, Nov. 2014 (invited from paper E62).

Δ25. D. Diamantopoulos, S. Xydis, K. Siozios and D. Soudris, "*Mitigating Memory-induced Dark Silicon in Many-Accelerator Architectures*", IEEE Computer Architecture Letters, Vol. 14, No. 2, pp. 136–139, 2015.

Δ26. K. Maragos, K. Siozios and D. Soudris, "*An Evolutionary Algorithm for Netlist Partitioning Targeting 3-D FPGAs*", IEEE Embedded System Letters, Vol. 7, No. 4, pp. 117–120, Sept. 2015.

Δ27. K. Siozios and D. Soudris, "*A Customizable Framework for Application Implementation onto 3-D FPGAs*", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, DOI: 10.1109/TCAD.2016.2529421

Δ28. P. Danassis, K. Siozios and D. Soudris, "*ANT3D: Simultaneous Partitioning and Placement for 3-D FPGAs based on Ant Colony Optimization*", in IEEE Embedded Systems Letters, Vol. 8, No. 2, pp. 41–44, 2016.

Δ29. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios, G. Economakos and D. Soudris. "*An Integrated Exploration and Virtual Platform Framework for Many-Accelerator Heterogeneous Systems*", ACM Transactions on Embedded Computing Systems (TECS), Vol. 15, No. 3, Article 43, 26 pages, March 2016 (invited from paper E70).

Δ30. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios, G. Economakos and D. Soudris, "*A Framework for Interconnection-Aware Domain-Specific Many-Accelerator Synthesis*", ACM Transactions on Embedded Computing Systems (TECS), Vol. 15, No. 3, Article 43, 26 pages, March 2016 (invited from paper E81).

Πρακτικά Διεθνών Συνεδρίων

E1. K. Tatas, K. Siozios, D. Soudris and A. Thanailakis, "*Power-Efficient Implementations of Multimedia Applications on Reconfigurable Platforms*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 1032-1035, Sep. 2003, Lisbon, Portugal.

E2. K. Tatas, K. Siozios, D. Soudris, K. Masselos, K. Potamianos, S. Blionas and A. Thanailakis, "*Power Optimization Methodology for Multimedia Applications Implementation on Reconfigurable Platforms*", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 430–439, Sep. 2003, Torino, Italy.

E3. K. Tatas, K. Siozios, N. Vassiliadis, D. J. Soudris, S. Nikolaidis, S. Siskos and A. Thanailakis, "*FPGA Architecture Design and Toolset for Logic Implementation*", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 607–616, Sep. 2003, Torino, Italy.

E4. V. Kalenteridis, H. Pournara, K. Siozios, K. Tatas, I. Pappas, S. Nikolaidis, S. Siskos, D. J. Soudris and A. Thanailakis, "*An Integrated FPGA Design Framework: Custom Designed FPGA Platform and Application Mapping Toolset Development*", Reconfigurable Architectures Workshop (RAW), pp. 138–145, April 2004, Santa Fe, New Mexico, USA.

E5. K. Siozios, G. Koutroumpezis, K. Tatas, D. Soudris, and A. Thanailakis, "*A Novel FPGA Configuration Bitstream Generation Algorithm and Tool Development*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 1116–1118, Aug. 2004, Antwerp, Belgium.

E6. D. Soudris, S. Nikolaidis, S. Siskos, K. Tatas, K. Siozios, G. Koutroumpezis, N. Vassiliadis, V. Kalenteridis, H. Pournara, I. Pappas, and A. Thanailakis, "*AMDREL: A Novel Low-Energy FPGA Architecture and Supporting CAD Tool Design Flow*", Asia South Pacific - Design Automation Conference (ASP-DAC) (Design Contest), pp. D3–D4, January 2005, Shanghai, China.

E7. K. Siozios, G. Koutroumpezis, K. Tatas, D. Soudris and A. Thanailakis, "*DAGGER: A Novel Generic Methodology for FPGA Bitstream Generation and its Software Tool Implementation*", Reconfigurable Architectures Workshop, (RAW), pp. 165b, Denver, April 2005, Colorado, USA.

E8. K. Siozios, K. Tatas, G. Koutroumpezis, D. Soudris, and A. Thanailakis, "*An Integrated Framework for Architecture Level Exploration of Reconfigurable Platform*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 658–661, Aug. 2005, Tampere, Finland.

E9. K. Siozios and D. Soudris, "*A Low-Energy FPGA: Architecture Design and Software-Supported Design Flow*", PhD Forum of International Conference of Field-Programmable Logic and Applications (FPL), pp. 707–708, Aug. 2005, Tampere, Finland.

E10. K. Siozios, G. Koutroumpezis, K. Tatas, N. Vassiliadis, V. Kalenteridis, H. Pournara, I. Pappas, D. Soudris, S. Nikolaidis, S. Siskos, and A. Thanailakis, "*The AMDREL Project in Retrospective*", IFIP International Conference on Very Large Scale Integration (VLSI-SoC), Oct. 2005, Perth, Western Australia.

E11. K. Siozios, K. Tatas, D. Soudris and A. Thanailakis, "*A Novel Methodology for Designing High-Performance and Low-Energy FPGA Routing Architecture*", International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 224, Feb. 2006, Monterey, California.

E12. K. Siozios, K. Tatas, D Soudris and A. Thanailakis, "*Platform-based FPGA Architecture: Designing High-Performance and Low-Power Routing Structure for Realizing DSP Applications*", Reconfigurable Architectures Workshop (RAW), pp. 10, April 2006, Rhodes, Greece.

E13. K. Siozios, D. Soudris and A. Thanailakis, "*A Novel Methodology for Designing High-Performance and Low-Power FPGA Interconnection Targeting DSP Applications*", International Symposium on Circuits and Systems (ISCAS), pp. 4383–4386, May 2006, Kos, Greece.

E14. K. Siozios, D. Soudris and A. Thanailakis, "*Efficient Power Management Strategy of FPGAs Using a Novel Placement Technique*", IFIP International Conference on Very Large Scale Integration (VLSI-SoC), pp. 204–209, Oct. 2006, Nice, France.

E15. K. Siozios, D. Soudris and A. Thanailakis, "*Designing Alternative FPGA Implementations Using Spatial Data from Hardware Resources*", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 403–414, Sep. 2006, Montpellier, France.

E16. K. Siozios and D. Soudris, "*Wire Segment Length and Switch Box Co-Optimization for FPGA Architectures*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 1–4, Aug. 2006, Madrid, Spain.

E17. K. Siozios and D. Soudris, "*A Temperature-Aware Mapping Methodology for FPGAs*", International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 223, Feb. 2007, Monterey, California.

E18. K. Siozios, S. Mamagkakis, D. Soudris and A. Thanailakis, "*Designing Heterogeneous FPGAs with Multiple SBs*", International Workshop on Applied Reconfigurable Computing (ARC), pp. 91–96, March 2007, Rio de Janeiro, Brazil.

E19. K. Siozios and D. Soudris, "*A Novel Methodology for Temperature-Aware Placement and Routing of FPGAs*", IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 55–60, May 2007, Porto Alegre, Brazil.

E20. K. Siozios, K. Sotiriadis, V. Pavlidis, and D. Soudris, "*Exploring Alternative 3D FPGA Architectures: Design Methodology and CAD Tool Support*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 652–655, Aug. 2007, Amsterdam, Netherlands.

E21. K. Siozios, K. Sotiriadis, V. Pavlidis, and D. Soudris, "*A Software-Supported Methodology for Designing High-Performance 3D FPGA Architectures*", IFIP International Conference on Very Large Scale Integration (VLSI-SoC), pp. 54–59, Oct. 2007, Atlanta, USA.

E22. A. Bartzas, N. Skalis, K. Siozios and D. Soudris, "*Exploration of Alternative Topologies for Application-Specific 3D Networks-on-Chip*", Workshop on Application Specific Processors (WASP), Oct. 2007.

E23. K. Siozios and D. Soudris, "*An Efficient Approach for Managing Power Consumption Hotspots Distribution on 3D FPGAs*", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 439–448, Sep. 2008, Lisbon, Portugal (Invited Paper).

E24. K. Siozios, A. Papanikolaou and D. Soudris, "*A method and tool for early design/technology search-space exploration for 3D ICs*", IFIP International Conference on Very Large Scale Integration (VLSI-SoC), pp. 359–364, Oct. 2008, Rhodes, Greece.

E25. K. Siozios and D. Soudris, "*A Novel Algorithm for Temperature-Aware P&R on 3D FPGAs*", IFIP International Conference on Very Large Scale Integration (VLSI-SoC), pp. 309–314, Oct. 2008, Rhodes, Greece.

E26. K. Siozios and D. Soudris, "*Application-Domain Specific Reconfigurable FPGA Platform: A Hardware/Software Design Approach*", PhD Forum of IFIP International Conference on Very Large Scale Integration (VLSI-SoC), pp. 46–40, Oct. 2008, Rhodes, Greece.

E27. K. Siozios and D. Soudris, "*A Novel Methodology for Exploring Interconnection Architectures Targeting 3D FPGAs*", Workshop on Reconfigurable Computing (WRC), Jan. 2009, Paphos, Cyprus.

E28. K. Siozios, V. Pavlidis, and D. Soudris, "*A Software-Supported Methodology for Exploring Interconnection Architectures Targeting 3-D FPGAs*", Design, Automation and Testing in Europe (DATE), pp. 172–177, April 2009, Nice, France.

E29. K. Siozios, D. Soudris and G. Economakos, "*Three-Dimensional FPGA Architectures: A Shift Paradigm for Energy-Performance Efficient DSP Implementations*", International Conference on Digital Signal Processing (DSP), pp. 1–6, July 2009, Santorini, Greece.

E30. K. Siozios, D. Soudris and D. Pnevmatikatos, "*A Framework for Enabling Fault Tolerance in Reconfigurable Architectures*", International Workshop on Applied Reconfigurable Computing (ARC), pp. 257–268, Mar. 2010, Bangkok, Thailand.

E31. K. Siozios, D. Soudris and D. Pnevmatikatos, "*Fault-Free: A Framework for Supporting Fault Tolerance in FPGAs*", Workshop on Reconfigurable Computing (WRC), Jan. 2010, Pisa, Italy.

E32. A. Richard, D. Milojevic, F. Robert, A. Bartzas, A. Papanikolaou, K. Siozios and D. Soudris, "*Fast Design Space Exploration Environment Applied on NoC's for 3D-Stakced MPSoC's*", International Conference on Architecture of Computing Systems (ARCS), pp. 1–6, Feb. 2010, Hannover, Germany.

E33. K. Siozios, I. Anagnostopoulos and D. Soudris, "*A High-Level Mapping Algorithm Targeting 3D NoC Architectures with Multiple Vdd*", IEEE Annual Symposium on VLSI (ISVLSI), pp. 444–445, July 2010, Kefalonia, Greece.

E34. K. Siozios, D. Soudris and D. Pnevmatikatos, "*Towards supporting Fault-Tolerance in FPGAs*", IEEE Annual Symposium on VLSI (ISVLSI), pp. 446–447, July 2010, Kefalonia, Greece.

E35. H. Sidiropoulos, K. Siozios and D. Soudris, "*NAROUTO: An Open-Source Framework for Supporting Architecture-Level Exploration at Heterogeneous FPGAs*", International Conference on Electronics, Circuits, and Systems (ICECS), pp. 532–535, Dec. 2010, Athens, Greece.

E36. K. Siozios, I. Anagnostopoulos and D. Soudris, "*Multiple Vdd on 3D NoC Architectures*", International Conference on Electronics, Circuits, and Systems (ICECS), pp. 833–836, Dec. 2010, Athens, Greece.

E37. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Methodology and Tool Framework for Supporting Rapid Exploration of Memory Hierarchies in FPGAs*", Workshop on Reconfigurable Computing (WRC), Jan. 2011, Heraklion, Greece.

E38. E. Xanthopoulos-Sotiriou, G. Economacos, K. Siozios and D. Soudris, "*Systematic Synthesis of Multimode Reconfigurable RTL Components*", Workshop on Reconfigurable Computing (WRC), Jan. 2011, Heraklion, Greece.

E39. K. Siozios, D. Rodopoulos and D. Soudris, "*Quick_Hotspot: A Software Supported Methodology for Supporting Run-Time Thermal Analysis at MPSoC Designs*", Workshop Proceedings on International Conference on Architecture of Computing Systems (ARCS), Feb. 2011, Como, Italy.

E40. K. Siozios, D. Soudris, "*Trading Fault-Masking with Performance Overhead for FPGAs*", Workshop Proceedings on International Conference on Architecture of Computing Systems (ARCS), pp. 7–10, Feb. 2011, Como, Italy.

E41. D. Diamantopoulos, K. Siozios, D. Bekiaris, and D. Soudris, "*A Novel Methodology for Architecture-Level Exploration of 3D SoCs*", Design & Technology of Integrated Systems in Nanoscale Era (DTIS), pp. 1–6, Apr. 2011, Athens, Greece.

E42. K. Siozios, A. Papanikolaou and D. Soudris, '"*CAD Tools for Designing 3D Integrated Systems*", IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2229–2232, May 2011, Rio de Janeiro, Brazil.

E43. M. Hubner, P. Figuli, R. Girardey, D. Soudris, K. Siozios and J. Becker, "*A Heterogeneous Multicore System on Chip with Run-Time Reconfigurable Virtual FPGA Architecture*", Reconfigurable Architectures Workshop (RAW), pp. 143–149, May 2011, USA.

E44. D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, "*Thermal optimization for micro-architectures through selective block replication*", International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), pp.59–66, July 2011, Samos, Greece.

E45. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Methodology and Tool Framework for Supporting Rapid Exploration of Memory Hierarchies in FPGAs*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 238–243, Sept. 2011, Chania, Greece.

E46. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Framework for Architecture-level Exploration of Communication Intensive Applications onto 3-D FPGAs*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 30–33, Sept. 2011, Chania, Greece.

E47. K. Siozios, D. Diamantopoulos, I. Kostavelis, E. Boukas, L. Nalpantidis, D. Soudris, A. Gasteratos, M. Avilés and I. Anagnostopoulos, "*SPARTAN Project: Efficient Implementation of Computer Vision Algorithms onto Reconfigurable*

Platform Targeting to Space Applications", International Workshop on Reconfigurable Communication Centric Systems-on-Chip (ReCoSoC), pp. 1–9, Jun. 2011, Montpellier, France (invited paper).

E48. M. Aviles, K. Siozios, D. Diamantopoulos, L. Nalpantidis, I. Kostavelis, E. Boukas, D. Soudris and A. Gasteratos, "*A Co-design Methodology for Implementing Computer Vision Algorithms for Rover Navigation onto Reconfigurable Hardware*", Workshop on Computer Vision on Low-Power Reconfigurable Architectures (during International Conference on Field-Programmable Logic and Applications), Sept. 2011, Chania, Greece.

E49. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Framework for Architecture-Level Exploration of 3-D FPGA Platforms*", International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 298–307, Sept. 2011, Madrid, Spain.

E50. K. Siozios and Dimitrios Soudris, "*Low-cost fault tolerant targeting FPGA devices*", Workshop on Reconfigurable Computing (WRC), Jan. 2012, Paris, France.

E51. H. Sidiropoulos, K. Siozios and D. Soudris, "*On Supporting Efficient Implementation of Communication-Intensive Applications onto 3D FPGAs*", Workshop on Reconfigurable Computing (WRC), Jan. 2012, Paris, France.

E52. H. Sidiropoulos, K. Siozios, P. Figuli, D. Soudris and M. Hubner, "*On Supporting Efficient Partial Reconfiguration with Just-In-Time Compilation*", Reconfigurable Architectures Workshop (RAW), pp. 328–335, May 2012, Shanghai, China (best paper award).

E53. K. Siozios and D. Soudris, "*A low-cost fault tolerant solution targeting to commercial FPGA devices*", NASA/ESA Conference on Adaptive Hardware and Systems (AHS), pp. 46–53, Jun. 2012, Erlangen, Germany.

E54. D. Diamantopoulos, K. Siozios, G. Lentaris, D. Soudris and M. Aviles Rodrigalvarez, "*SPARTAN Project: On Profiling Computer Vision Algorithms for Rover Navigation*", NASA/ESA Conference on Adaptive Hardware and Systems (AHS), pp. 174–181, Jun. 2012, Erlangen, Germany.

E55. G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris and M. Aviles, "*Hardware Implementation of Stereo Correspondence Algorithm for the ExoMars Mission*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 667–670, Aug. 2012, Oslo, Norway.

E56. K. Siozios, H. Sidiropoulos, D. Diamantopoulos, P. Figuli, D. Soudris, M. Hubner and J. Becker, "*On Designing Self-Aware Reconfigurable Platforms*", Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS), pp. 14–17, Aug. 2012, Oslo, Norway.

E57. G. Lentaris, D. Diamantopoulos, G. Stamoulias, K.Siozios, D.Soudris and M. Avilés Rodrigálvarez, "*FPGA-based Path-planning of High Mobility Rover for Future Planetary Missions*", IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp. 85–88, Dec. 2012, Seville, Spain.

E58. G. Lentaris, D. Diamantopoulos, K. Siozios, I. Stamoulias, I. Kostavelis, E. Boukas, L. Nalpantidis, D. Soudris, A. Gasteratos, and M. Aviles, "*SPARTAN: Efficient Implementation of Computer Vision Algorithms for Autonomous Rover Navigation*", Workshop on Reconfigurable Computing (WRC), Jan. 2013, Berlin, Germany.

E59. G. Lentaris, I. Stamoulias, D. Diamantopoulos, K. Siozios, and D. Soudris, "*An FPGA implementation of the SURF algorithm for the ExoMars programme*", Workshop on Reconfigurable Computing (WRC), Jan. 2013, Berlin, Germany.

E60. D. Diamantopoulos, K. Siozios, and D. Soudris, "*A Framework for Performing Fault-Tolerant Placement Based on Genetic Algorithm*", Workshop on Reconfigurable Computing (WRC), Jan. 2013, Berlin, Germany.

E61. D. Diamantopoulos, K. Siozios, S. Xydis and D. Soudris, "*A Framework for Supporting Parallel Application Placement onto Reconfigurable Platforms*", Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (PARMA), Jan. 2013, Berlin, Germany.

E62. D. Diamantopoulos, K. Siozios, E. Sotiriou-Xanthopoulos, G. Economakos and D. Soudris, "*HVSoCs: A Framework for Rapid Prototyping of 3-D Hybrid Virtual System-on-Chips*", IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pp. 2194–2199, May 2013, Cambridge, MA.

E63. K. Siozios, D. Soudris and M. Hubner, "*On Supporting Adaptive Fault Tolerant at Run-Time with Virtual FPGAs*", IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pp. 2206–2211, May 2013, Cambridge, MA.

E64. E. Sotiriou-Xanthopoulos, K. Siozios, G. Economakos and D. Soudris, "*A Process-Based Reconfigurable SystemC Module for Simulation Speedup*", International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), pp. 72–79, July 2013, Samos, Greece.

E65. H. Sidiropoulos, P. Figuli, K. Siozios, D. Soudris and J. Becker, "*A platform-independent runtime methodology for mapping multiple applications onto fpgas through resource virtualization*", International Conference on Field-Programmable Logic and Applications (FPL), pp. 1-4, Sept. 2013, Porto, Portugal.

E66. E. Xanthopoulos-Sotiriou, S. Xydis, K. Siozios, G. Economakos and D. Soudris, "*Effective Platform-Level Exploration for Heterogeneous Multicores Exploiting Simulation-Induced Slacks*", Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM), pp. 13-16, Jan. 2014, Vienna, Austria.

E67. H. Sidiropoulos, K. Siozios and D. Soudris, "*A Framework for Mapping Dynamic Virtual Kernels onto Heterogeneous Reconfigurable Platforms*", IEEE International Parallel & Distributed Processing Symposium Workshops (IPDPSW), pp. 170-175, May 2014, Phoenix, USA.

E68. K. Siozios, D. Soudris and M. Hubner, "*A Framework for Customizing Virtual 3-D Reconfigurable Platforms at Run-Time*", IEEE International Parallel & Distributed Processing Symposium Workshops (IPDPSW), pp. 183-188, May 2014, Phoenix, USA.

E69. N. Zompakis and K. Siozios, "*A Framework for Reducing the Modeling and Simulation Complexity of Cyberphysical Systems*", Workshop on Virtual Prototyping of Parallel and Embedded Systems (VIPES), pp. 360–365, July 2014, Samos, Greece.

E70. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios and G. Economakos, "*Co-Design of Many-Accelerator Heterogeneous Systems Exploiting Virtual Platforms*", International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), pp. 1–8, July 2014, Samos, Greece.

E71. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios, G. Economakos and D. Soudris, "*Hardware Accelerated Rician Denoise Algorithm for High Performance Magnetic Resonance Imaging*", International Conference on Wireless Mobile Communication and Healthcare (MOBIHEALTH), pp. 222-225, Nov. 2014, Athens, Greece.

E72. K. Siozios, P. Figuli, H. Sidiropoulos, C. Tradowsky, K. Maragos, S. P. Delicia, D. Soudris and J. Becker, "*TEAChER: TEach AdvanCEd Reconfigurable architectures and tools*", International Workshop on Applied Reconfigurable Computing (ARC), pp. 103–114, Apr. 2015, Bochum, Germany.

E73. D. Diamantopoulos, I. Galanis, K. Siozios, G. Economakos and D.Soudris, "*A Framework for Rapid System-Level Synthesis Targeting to Reconfigurable Platforms: A Computer Vision Case Study*", International Workshop on Reconfigurable Computing (WRC), Jan. 2015, Amsterdam, Netherlands.

E74. K. Maragos, K. Siozios and D. Soudris, "*A Genetic Algorithm based Partitioning for 3-D Reconfigurable Architectures*", Workshop on Reconfigurable Computing (WRC), Jan. 2015, Amsterdam, Netherlands.

E75. P. Figuli, C. Tradowsky, J. A. Lucio Martinez, H. Sidiropoulos, K. Siozios, H. Stenschke, D. Soudris, and J. Becker, "*A Novel Concept for Adaptive Signal Processing on Reconfigurable Hardware*", International Workshop on Applied Reconfigurable Computing (ARC), pp. 311–320, Apr. 2015, Bochum, Germany.

E76. D. Diamantopolous, S. Xydis, K. Siozios and D. Soudris, "*Dynamic Memory Management in Vivado-HLS for Scalable Many-Accelerator Architectures*", International Workshop on Applied Reconfigurable Computing (ARC), pp. 117–128, Apr. 2015, Bochum, Germany.

E77. G. Lentaris, I. Stamoulias, D. Diamantopoulos, K. Maragos, K. Siozios, D. Soudris, M. Aviles Rodrigalvarez, M. Lourakis, X. Zabulis, I. Kostavelis, L. Nalpantidis, E. Boukas and A. Gasteratos, "*SPARTAN/SEXTANT/COMPASS: Advancing Space Rover Vision via Reconfigurable Platforms*", International Workshop on Applied Reconfigure Computing (ARC), pp. 475–486, Apr. 2015, Bochum, Germany.

E78. D. Diamantopoulos, S. Xydis, K. Siozios and D. Soudris, "*High-Level-Synthesis extensions for scalable Single-Chip Many-Accelerators on FPGAs*", International Conference in Field-Programmable Logic and Applications (FPL), pp.1–2, Sept. 2015, London, England.

E79. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios, G. Economakos and D. Soudris, "*Rapid prototyping and Design Space Exploration methodologies for many-accelerator systems*", International Conference in Field-Programmable Logic and Applications (FPL), pp. 1–2, Sept. 2015, London, England.

E80. E. Sotiriou-Xanthopoulos, G. Shalina, P. Figuli, K. Siozios, G. Economakos, J. Becker, "*A Power Estimation Technique for Cycle-Accurate Higher-Abstraction SystemC-based CPU Models*", International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pp. 70–77, July 2015, Samos, Greece.

E81. E. Sotiriou-Xanthopoulos, S. Xydis, K. Siozios and G. Economakos, "*A virtual platform for exploring hierarchical interconnectio for many-accelerator systems*", International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pp. 384–389, July 2015, Samos, Greece.

E82. P. Danassis, K. Siozios and D. Soudris, "*Parallel Application Placement onto 3-D Reconfigurable Architectures*", International Conference on Modern Circuits and Systems Technologies (MOCAST), pp. 1–5, May 2016, Thessaloniki, Greece.

E83. E. Sotiriou-Xanthopoulos, L. Masing, K. Siozios, G. Economakos, D. Soudris, J. Becker, "*An OpenCL-based Framework for Rapid Virtual Prototyping of Heterogeneous Architectures*", In Virtual Prototyping of Parallel and Embedded Systems (VIPES), July 2016, Samos, Greece.

E84. K. Siozios, I. Savvidis and D. Soudris, "*A Framework for Exploring Alternative Fault-Tolerant Schemes Targeting 3-D Reconfigurable Architectures*", Int. Conf. on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), July 2016, Samos, Greece.

Οι εργασίες E1-E84 έχουν γίνει δεκτές για παρουσίαση ύστερα από κρίση σε πρακτικά διεθνών συνεδρίων.

Ζ. Πρακτικά Εθνικών Συνεδρίων με Κριτές

Z1. A. Karakos and K. Siozios, "*Secure Networking Using Mobile IP*", Panhellenic Conference on Informatics (PCI), pp. 284–293, Nov. 2001, Nicosia, Cyprus.

Z2. K. Siozios, P. Efraimidis and A. Karakos, "*Design and implementation of a Secure Mobile IP Architecture*", Panhellenic Conference in Informatics (PCI), pp. 269–279, Nov. 2003, Thessaloniki, Greece.

Z3. I. Pappas, N. Vassiliadis, V. Kalenteridis, H. Pournara, S. Nikolaidis, S. Siskos, K. Siozios, G. Koutroumpezis, K. Tatas, D. J. Soudris, A. Thanailakis, "*Fine-Grain Reconfigurable Platform: FPGA Hardware Design and Software Toolset Development*", Proceedings of Microelectronics Microsystems and Nanotechnology, Nov. 2004, Greece.

Z4. K. Siozios, K. Sotiriadis and D. Soudris, "*MEANDER: A CAD Tool Framework for Designing 2D/3D FPGAs*", International Conference "Micro&Nano2007" on Micro- Nanoelectronics, Nanotechnology and MEMs, pp. 119, Nov. 2007, Athens, Greece.

Z5. D. Diamantopoulos, G. Lentaris, A. Douklias, K.Siozios, D.Soudris and M. Avilεs Rodrigαlvarez, "*The SPARTAN Project: FPGA-based Implementation of Computer Vision Algorithms Targeting to Space Applications*", PAnhellenic Conference on Electronics and Telecommunications (PACET), 2012, Thessaloniki, Greece.

Οι παραπάνω εργασίες έχουν γίνει δεκτές για παρουσίαση ύστερα από κρίση σε πλήρη κείμενο (full paper).

Η. Συμμετοχή σε Workshops χωρίς κριτές (poster presentations)

H1. K. Siozios, A. Papanikolaou, A. Bartzas and D. Soudris, "*System-Level Exploration of 3-D Interconnection Schemes*", Friday Workshop on 3D Integration at Design, Automation and Testing in Europe (DATE), April 2009, Nice, France.

H2. A. Bartzas, K. Siozios, and D. Soudris, "*Topology Exploration and Buffer Sizing for Three-Dimensional Networks-on-Chip*", Friday Workshop on 3D Integration, Design, Automation and Testing in Europe (DATE), April 2009, Nice, France.

H3. K. Tatas, C. Kyriacou, A. Bartzas, K. Siozios and D. Soudris, "*A Novel NoC Architecture Framework for 3D Chip MPSoC Implementations*", Friday Workshop on 3D Integration, Design, Automation and Testing in Europe (DATE), 2010, Dresden, Germany.

H4. D. Diamantopoulos, G. Lentaris, K. Siozios, D. Soudris and M. Aviles, "*Towards Accelarating Computer Vision Algorithms Targeting to Space Applications with a Heterogeneous Platform*", Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Design, Automation and Testing in Europe (DATE), 2012, Dresden, Germany.

H5. K. Tatas, C. Kyriacou, K. Siozios, A. Bartzas and D. Soudris, "*SYSMANTIC: A 3D NoC MPSoC Architecture Exploration and Implementation Framework*", Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Design, Automation and Testing in Europe (DATE), 2012, Dresden, Germany.

H6. H. Sidiropoulos, K. Siozios and D. Soudris, "*Rapid architecture-level exploration of 2D and 3D heterogeneous FPGA architectures*", Friday Workshop (at DATE Conference) on Reconfigurable Computing V2.0: The Next Gerneration of Technology, Architectures and Design Tools (ConfigComp), March 22, 2013, Grenoble, France.

H7. D. Diamantopoulos, K. Siozios, J. Stamoulias, G. Lentaris, D. Soudris and M. Aviles, "*Towards Computer Vision FPGA Acceleration*", Friday Workshop (at DATE Conference) on Reconfigurable Computing V2.0: The Next Gerneration of Technology, Architectures and Design Tools (ConfigComp), March 22, 2013, Grenoble, France.

V. ΠΑΡΟΥΣΙΑΣΗ ΕΡΓΑΣΙΩΝ ΣΕ ΔΙΕΘΝΗ ΣΥΝΕΔΡΙΑ

- 8^{th} Panhellenic Conference in Informatics, 2001, Nicosia, Cyprus (present paper Z1).
- 13th International Conference on Field-Programmable Logic and Applications (FPL), 2003, Lisbon, Portugal (present paper E1).
- 9th Panhellenic Conference in Informatics, 2003, Thessaloniki, Greece (present paper Z2).

- 15th International Conference on Field-Programmable Logic and Applications (FPL), 2005, Tampere, Finland (present papers E8 and E9).
- 14th International Symposium on Field-Programmable Gate Arrays (FPGA), 2006, Monterey, California, USA (present paper E11).
- 13th Reconfigurable Architectures Workshop (RAW), 2006, Rhodes, Greece (present paper E12).
- 4th PhD Forum during the Design, Automation and Test in Europe (DATE), 2006, Munich, Germany.
- IEEE International Symposium on Circuits and Systems (ISCAS), 2006, Kos, Greece (present paper E13).
- 16th International Conference on Field-Programmable Logic and Applications (FPL), 2006, Madrid, Spain (present paper E16).
- 5th PhD Forum during the Design, Automation and Test in Europe (DATE), 2007, Nice, France.
- 15th International Symposium on Field-Programmable Gate Arrays (FPGA), 2007, Monterey, California, USA (present paper E17).
- 18th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2008, Lisbon, Portugal (present paper E23).
- Workshop on Reconfigurable Computing (WRC), 2009, Paphos, Cyprus (present paper E27).
- Design, Automation and Testing in Europe (DATE), 2009, Nice, France (present papers E28 and H1).
- PhD Forum during the D43D: System Design for 3D Silicon Integration Workshop, June 17-18, 2009, MINATEC, Grenoble, France.
- Workshop on Reconfigurable Computing (WRC), 2010, Pisa, Italy (present paper E31).
- 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Athens, Greece, 2010 (present paper E35).
- Workshop on Reconfigurable Computing (WRC), 2011, Heraklion, Greece (present paper E37).
- Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (co-located with International Conference on Architecture of Computing Systems), Feb. 22, 2011 (present paper E39).
- Workshop on Software-Controlled, Adaptive Fault-Tolerance in Microprocessors (SCAFT) (co-located with International Conference on Architecture of Computing Systems), Feb. 22, 2011 (present paper E40).
- IEEE International Symposium on Circuits and Systems (ISCAS), pp. 2229-2232, May 15-18, 2011, Rio de Janeiro, Brazil (present paper E42).
- International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), Samos, Greece, July 2011 (present paper E44).
- International Conference on Field-Programmable Logic and Applications (FPL), Greece, September 2011 (present papers E45 and E46).
- Workshop on Computer Vision on Low-Power Reconfigurable Architectures, International Conference on Field-Programmable Logic and Applications, Greece, September 2011 (present paper E48).
- Workshop on Reconfigurable Computing (WRC), 2012, Berlin, Germany (present papers E58, E59 and E60).
- Workshop on Virtual Prototyping of Parallel and Embedded Systems (VIPES), held in conjunction to the IPDPS 2013 conference, May 2013 (present papers E62 and E63).

VI. ΔΙΔΑΚΤΙΚΟ ΚΑΙ ΕΚΠΑΙΔΕΥΤΙΚΟ ΕΡΓΟ

2005–2006 Συστήματα VLSI-II (Εργαστηριακές και φροντιστηριακές ασκήσεις)
Τμήμα Ηλεκτρολόγων Μηχανικών και Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης.

2006–2007 Συστήματα VLSI-II (Εργαστηριακές και φροντιστηριακές ασκήσεις)
Τμήμα Ηλεκτρολόγων Μηχανικών και Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης.

2006–2007 Μικροηλεκτρονική-ΙΙ (Εργαστηριακές και φροντιστηριακές ασκήσεις)
Τμήμα Ηλεκτρολόγων Μηχανικών και Μηχανικών Η/Υ, Δημοκρίτειο Πανεπιστήμιο Θράκης.

2008–2014 Ψηφιακά Συστήματα VLSI (Εργαστηριακές και φροντιστηριακές ασκήσεις)
Σχολή Ηλεκτρολόγων Μηχανικών και Μηχανικών Η/Υ, Εθνικό Μετσόβιο Πολυτεχνείο.

2005–2006 Πληροφορική-ΙΙ (Εργαστήριο Λειτουργικών Συστημάτων)
Εργαστηριακός συνεργάτης (6 ώρες/εβδομάδα), *Τμήμα Βιομηχανικού Σχεδιασμού, Τ.Ε.Ι. Δυτικής Μακεδονίας*.

2006–2007 Πληροφορική-Ι (Θεωρία)
Εργαστηριακός συνεργάτης (2 ώρες εβδομαδιαίως), *Τμήμα Βιομηχανικού Σχεδιασμού, Τ.Ε.Ι. Δυτικής Μακεδονίας*.

2009–2010 Αρχιτεκτονική Η/Υ (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2009-2010 Δίκτυα Η/Υ (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2010–2011 Ψηφιακός Αυτόματος Έλεγχος (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2010–2011 Τοπικά Δίκτυα Αεροσκαφών (Θεωρία)
Επιστημονικός συνεργάτης (3 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2010–2011 Μικροϋπολογιστές (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2011–2012 Δομημένος Προγραμματισμός (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2011–2012 Αρχιτεκτονική Η/Υ (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2011–2012 Δίκτυα Η/Υ (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2011–2012 Ψηφιακή Σχεδίαση ΙΙ (Θεωρία)
Διδάσκοντας με το Π.Δ. 407/80, *Τμήμα Μηχανικών Πληροφορικής & Τηλεπικοινωνιών, Πανεπιστήμιο Δυτικής Μακεδονίας*.

2012–2013 Εισαγωγή στα Ηλεκτρονικά (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Εισαγωγή στα Ηλεκτρονικά (Εργαστήριο)
Εργαστηριακός συνεργάτης (8 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Ηλεκτρονικά Τηλεπικοινωνιών (Εργαστήριο)
Εργαστηριακός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Συστήματα Ψηφιακής Επεξεργασίας Σήματος (Θεωρία)
Έκτακτος εκπαιδευτικός (3 ώρες/εβδομάδα), *Διατμηματικό/Διαπανεπιστημιακό Μεταπτυχιακό, Εθνικό και Καποδιστριακό Πανεπιστήμιο Αθηνών*.

2012–2013 Ψηφιακά Συστήματα (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Ψηφιακά Συστήματα (Εργαστήριο)
Εργαστηριακός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Μικροϋπολογιστές (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Μικροϋπολογιστές (Εργαστήριο)
Εργαστηριακός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2012–2013 Αντικειμενοστραφής Προγραμματισμός Η/Υ (Θεωρία)
Επιστημονικός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Αυτοματισμού, Τ.Ε.Ι. Χαλκίδας*.

2013–2014 Ηλεκτρικές Μηχανές (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2013–2014 Ηλεκτρικές Μηχανές (Εργαστήριο)
Εργαστηριακός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2013–2014 Ηλεκτρονικά Ισχύος (Θεωρία)
Επιστημονικός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2013–2014 Ηλεκτρονικά Ισχύος (Εργαστήριο)
Εργαστηριακός συνεργάτης (2 ώρες/εβδομάδα), *Τμήμα Τεχνολογίας Αεροσκαφών, Τ.Ε.Ι. Χαλκίδας*.

2013–2014 Δομή και Λειτουργία Μικροϋπολογιστών (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Αυτοματισμού, ΤΕΙ Πειραιά*.

2013–2014 Συστήματα Ψηφιακής Επεξεργασίας Σήματος (Θεωρία)
Έκτακτος εκπαιδευτικός (3 ώρες/εβδομάδα), *Διατμηματικό/Διαπανεπιστημιακό Μεταπτυχιακό, Εθνικό και Καποδιστριακό Πανεπιστήμιο Αθηνών*.

2014–2015 Αρχιτεκτονική Υπολογιστών (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2014–2015 Λειτουργικά Συστήματα Ι (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2014–2015 Προγραμματισμός Υπολογιστών (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2014–2015 Ψηφιακή Σχεδίαση (Εργαστήριο)
Εργαστηριακός συνεργάτης (8 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2015–2016 Λειτουργικά Συστήματα Ι (Εργαστήριο)
Εργαστηριακός συνεργάτης (6 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2015–2016 Ψηφιακή Σχεδίαση (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

2015–2016 Σχεδίαση Ψηφιακών Συστημάτων (Εργαστήριο)
Εργαστηριακός συνεργάτης (4 ώρες/εβδομάδα), *Τμήμα Μηχανικών Πληροφορικής, Τ.Ε.Ι. Αθήνας*.

VII. ΔΙΕΘΝΗΣ ΑΝΑΓΝΩΡΙΣΗ

Α. Διεθνή Βραβεία

- 4^{th}θέση στο Διεθνή Διαγωνισμό (Design Contest) στα πλαίσια του Συνεδρίου ASP-DAC 2005 (Asia South Pacific – Design Automation Conference) January 18-21, 2005, Shanghai, China για τον σχεδιασμό (έμφαση στο λογισμικό) που πραγματοποιήθηκε στα πλαίσια του Ερευνητικού Ευρωπαϊκού Προγράμματος "*AMDREL: Architectures and Methodologies for Dynamic REconfigurable Logic*" IST-2001-34379, με χρηματοδότηση από την Ευρωπαϊκή Ένωση στα πλαίσια του 5th IST Framework.
- Award "*Honorable mention for design contest entry*" for your design "*AMDREL: A novel low-energy FPGA architecture and supporting CAD tool design flow*" submitted for VLSI Design, 2005 Design Contest of 18th Int. Conference on VLSI 2005 January 3-5, 2005, Taj Bengal, Kolkata, India. Το βραβείο αφορά μέρος των αποτελεσμάτων (έμφαση στο υλικό) του Ερευνητικού Ευρωπαϊκού Προγράμματος AMDREL: "Architectures and Methodologies for Dynamic REconfigurable Logic" IST-2001-34379, με χρηματοδότηση από την Ευρωπαϊκή Ένωση στα πλαίσια του 5th IST Framework.
- Best paper award για την εργασία E52 (H. Sidiropoulos, K. Siozios, P. Figuli, D. Soudris and M. Hubner, "*On Supporting Efficient Partial Reconfiguration with Just-In-Time Compilation*", Reconfigurable Architectures Workshop (RAW), May 2012, China).
- 2ο βραβείο με χρηματική αμοιβή στον διαγωνισμό της Cadence (Cadence Design Contest 2013) για την το περιβάλλον γρήγορης και αξιόπιστης ανάπτυξης ψηφιακών εφαρμογών σε υλικό με τη διακριτική ονομασία Plug&Chip.

Β. Οργάνωση Summer School

- 1^{st} Pandora Summer School: "Progression and Diversity of Reconfigurable Architectures and Tools", 14-19/09/2016, National Technical University of Athens (N.T.U.A.), Greece.
- 2^{nd} Pandora Summer School: "Progression and Diversity of Reconfigurable Architectures and Tools", 19-23/09/2016, Karlsruhe Institute of Technology (K.I.T.), Germany.

Γ. Συμμετοχή στην Οργάνωση Επιστημονικών Συνεδρίων

1. Υπεύθυνος Συνεδρίας (Session Chair) του 10th International Workshop Power and Timing Modeling, Optimization and Simulation (PATMOS), Lisbon, Portugal, 10-12 Sept. 2008.
2. Μέλος της επιτροπής (Program Committee) στο 17th Reconfigurable Architectures Workshop (RAW), Atlanta, USA, 2010.

3. Μέλος της επιτροπής (Program Committee) στο International Symposium on Electronic System Design (ISED), India, 2011.
4. Publicity chair, 6th HiPEAC Workshop on Reconfigurable Computing (WRC), January 2012.
5. Μέλος της επιτροπής (Program Committee) στο 7th International Workshop on Reconfigurable Computation-centric Systems-on-Chip (ReCoSoC), York, UK, 2012.
6. 4th IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms (M2A2 2012), July 10-13, 2012, Madrid, Spain.
7. Μέλος της επιτροπής (Program Committee) στο International Symposium on Electronic System Design (ISED), India, 2012.
8. Μέλος της επιτροπής (Program Committee) στο 10th IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA), 2012, Madrid, Spain.
9. Μέλος της επιτροπής (Program Committee) στο 8th International Workshop on Reconfigurable Computation-centric Systems-on-Chip (ReCoSoC), Germany, 2013.
10. Μέλος της επιτροπής (Program Committee) στο International Symposium on Electronic System Design (ISED), Singapore, 2013.
11. Μέλος της επιτροπής (Program Committee) στο 5th IEEE Workshop on Multicore and Multithreaded Architectures and Algorithms (M2A2),Melbroune, Australia, 2013.
12. Μέλος της επιτροπής (Program Committee) στο 9th International Workshop on Reconfigurable Computation-centric Systems-on-Chip (ReCoSoC), Montpellier, France, 2014.
13. Μέλος της επιτροπής (Program Committee) στο 6th IEEE Workshop on Multicore and Multithreaded Architectures and Algorithms (M2A2), Paris, France, 2014.
14. Μέλος της επιτροπής (Program Committee) στο 10th International Workshop on Reconfigurable Computation-centric Systems-on-Chip (ReCoSoC), Bremen, Germany, 2015.
15. The 7th IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms, New York, USA, 2015.
16. Μέλος της επιτροπής (Program Committee) στο 17th IEEE International Conference on High Performance and Communications (HPCC), New York, USA, 2015.
17. Μέλος της επιτροπής (Program Committee) στο International Conference on Modern Circuits and Systems Technologies (MOCAST), Thessaloniki, Greece, 2016.
18. Μέλος της επιτροπής (Program Committee) στο 11th International Workshop on Reconfigurable Computation-centric Systems-on-Chip (ReCoSoC), Tallin, Estonia, 2016.

Δ. Κριτής Εργασιών σε Περιοδικά και Συνέδρια

Περιοδικά:

- IEEE Transactions on VLSI (TVLSI)
- IEEE Transactions on Nanotechnology
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Embedded Systens (TECS)
- ACM Transactions on Reconfigurable Computing (TRETS)
- VLSI Design, Hindawi Publishing Corporation
- Journal of Circuits Systems and Computers
- IEEE Transactions on Industrial Informatics
- IEEE Embedded System Letters
- Elsevier, Journal of System Architectures (JSA)
- Journal of Circuits, Systems, and Computers

Συνέδρια:

- Design, Automation and Test in Europe (DATE)
- Field-Programmable Logic and Applications (FPL)
- IEEE International Symposium on Circuits and Systems (ISCAS)
- International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)
- Power And Timing Modeling, Optimization and Simulation (PATMOS)
- Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES)
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)
- Great Lakes Symposium on VLSI (GLS-VLSI)
- Asia Symposium on Quality Electronic Design (ASQED)
- IEEE International Conference on Electronics, Circuits and Systems (ICECS)
- Workshop on Reconfigurable Computing (WRC)
- International Conference on Modern Circuits and Systems Technologies (MOCAST)
- International Symposium on Embedded Computing and System Design (ISED)

VIII. ΔΙΕΘΝΕΙΣ ΕΠΙΣΤΗΜΟΝΙΚΕΣ ΕΝΩΣΕΙΣ

- Μέλος του Institute of Electrical and Electronic Engineering (IEEE).
- Μέλος του Τεχνικού Επιμελητηρίου Ελλάδος (ΤΕΕ).
- Μέλος του Πανελληνίου Συλλόγου Διπλωματούχων Μηχανολόγων Ηλεκτρολόγων.
- Κάτοχος της άδειας άσκησης επαγγέλματος του Ηλεκτρολόγου Μηχανικού και Μηχανικού Υπολογιστών.