Curriculum Vitae

Thomas Noulis

Personal Data

Date of birth	July 4th, 1980
Place of birth	Thessaloniki, Greece
Home Address	Xanthou 3, 55535 Pilea - Thessaloniki, Greece
Marital Status	Married with one child
Phone number	Office GR +302310998774
e-mail	tnoul@physics.auth.gr , t.noulis@gmail.com,

Occupation

- Faculty Member / Electronics Laboratory – Physics Department - Aristotle University of Thessaloniki

Education

03/2006 –05/2009	**Ph.D** Dissertation on the "Design of Integrated circuits for signal processing", Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki, (in collaboration with LAAS-CNRS, Toulouse, France)
09/2003 – 10/2005	**M.Sc**. Diploma in Electronics Engineering -Technology of Electronic Circuits Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki, CGPA: 9.61/10 (Honors Degree)
09/1998 – 11/2003	**B.Sc**. Degree in Physics (Option: Electronics & Telecommunications), Physics Department , Aristotle University of Thessaloniki, CGPA:7.32/10

Military Obligations Fulfilled with the field grade of a Sergeant

Professional Experience

A. Industry & Research Experience

April 2015 - present	Faculty Member- Lecturer – at Aristotle University of Thessaloniki – Greece, Physics Dept. Electronics Laboratory
April 2014 – April 2015	Senior Expert RFMS Engineer at INTEL MOBILE COMMUNICATIONS (IMC) GmbH / Wireless Platform R&D – Munich, Germany. ✓ Interface between RFMS Modeling and Product Design Groups of IMC ✓ RFMS Modeling and Simulation 28nm & 14nm technology nodes / Measurement and Testing ✓ 14nm Design methodology (Flow & EDA tooling) -Product migration/ porting analysis ✓ PDK concept definition on 14nm FinFET and 28nm CMOS tech nodes- simulation speed up, substrate crosstalk, self-heating, model validation, extraction /net list size minimization – modeling – simulation de-bugging, in-house inductor flow spec and coordination, PDK design documentation (14nm FinFET and 28nm CMOS PDKs) on modeling and device usage ✓ Training the US (Arizona and Oregon) Design teams on 14nm virtuoso Design Environment ✓ Signal and Noise Integrity / SiP and SoC modeling and flow unification / Dynamic IR Drop ✓ Tape-Out on C28 nm and c14 nm (circuit and mask design)
June 2012 to March 2014	Senior RFMS Engineer at INTEL MOBILE COMMUNICATIONS (IMC) GmbH / Wireless Platform R&D – Munich, Germany. ✓ Area estimation Analysis/Tooling – Product migration ✓ Signal and Noise Integrity / SiP and SoC modeling ✓ Analog/RF IC design for test and model validation - Passives/Actives Working Group Consulting- Passive in Package Innovation ✓ FoM process node/technology analysis ✓ TO on TSMC28nm, UMC28nm, Intel 14nm
Feb 2012 – March 2012	SoC Noise/Power Integrity Engineer and Project Lead - Scientific Consultant at HELIC Inc-Remote Work Contract (Freelance) ✓ Project Manager of Substrate Noise Analysis (SNA) EDA tool - Technical lead, project coordination and Technical Deliverable Writing – Signal and Noise Integrity ✓ Flow establishment, Modeling validation and testing coordination
July 2011 - Jan 2012	R&D Engineer & Analog/RF IC Designer for the Semiconductor Company HELIC Inc. – Athens R&D Center 1 (HQs) - R&D and IC Design Depts. ✓ Product Manager of Substrate Noise Analysis (SNA) EDA tool - Technical lead & project coordination ✓ Freescale FSL_SGPC project (28nm CMOS test shuttle) - substrate coupling analysis on 12 VCOs having different isolation schemes – measurements verification ✓ RF IC design (SNA PHORMINX chip lead (tsmc 65nm): technical lead from initial concept to chip implementation and chip measurement of an SNA related mixed signal chip (indicative circuitries - LNA, HF noise sensors, 80kGate noise transmitter CMOS logic) ✓ DieHARD chip – substrate modeling 'on wafer' validation structures (tsmc 65nm)
May 2008 – July 2011	R&D Engineer/ IC Designer for the Semiconductor Company HELIC Inc. – Thessaloniki R&D Center 2 - R&D and IC Design Depts.

	✓ RF/Analog IC design: Fujitsu Microelectronics project - design of a power amplifier (layout design) & OKI project – design of power amplifier (layout) \ ✓ PDK Compact Modeling benchmarking (fujitsu 90nm (BSIM4 and PSP) & 65nm CMOS, tsmc 65nm CMOS, Peregrine 0.25um SOS Ultra CMOS) ✓ Measurement and Validation – On wafer TEGs/ EDA tool validation ✓ TSMC substrate noise certification tests using a c56nm 2.27GHz VCO noise victim vehicle
Jan. 2008 – Oct. 2008	Analog IC designer in the framework of annual Scholarship (Honors) Research Program of Aristotle Univ. Research Committee, Aristotle Univ. of Thessaloniki (Project code 50120) ✓ Current mode Radiation detection Charge Sensitive CMOS (0.35um CMOS amd SiGe BiCMOS) Amplifier design
Nov. 2005 – July 2006	Analog IC Designer in the Project "Atomic Dosimetry using RADFETs", Electronics Lab., Physics Dept., Aristotle Univ. of Thessaloniki (PYTHAGORAS Project, Project Code 80877) ✓ Radiation dosimetry IC architectures using CMOS processes
April 2004 – Sept. 2005	Analog IC Designer in the Project "Sensor Interface Integrated Circuit Design for Space Application X-ray Spectroscopy", Electronics Lab., Physics Dept., Aristotle Univ. of Thessaloniki, scientific cooperation between GSRT-Greece and CNRS (LAAS) – France (PLATON Project, Project Code 10200) ✓ Radiation Detection front end IC electronics development: design and measurement of CMOS (0.35um and 0.6um) sensor interface microchips

B. Academic Experience

Mar. 2010 – Aug. 2010	Visiting Professor at the Physics Department of Aristotle University of Thessaloniki, Section of Electronics and Computers–Teaching staff at the 6th semester Lab. Course "Electronics Laboratory"
Oct. 2008 – Jun. 2009	Adjunct Professor in the Technical Educational Institute of Serres, in the Lab course "Analog Electronics", Department of Computer Science and Communications
Oct. 2006 – Feb. 2007	Adjunct Professor in the Technical Educational Institute of Serres, in the Lab courses "Electrical Circuits" and "Analog Electronics", Department of Computer Science and Communications
Oct. 2004 – Feb. 2005	Teaching staff in the Occupational Constitution Institute of Thermi (Thessaloniki) in the field of "Network administrating and Computers", in the 3rd semester Lab course "Communications Techniques"

Relevant Skills

- Project and Product management (Product manager of Noise/Signal Integrity EDA tools – Technical Lead)
- Excellent organization skills - attention to details / Proposals and Deliverables writing
- Analog and RF IC design, Radiation detection Integrated Circuit design for Particle Detection Applications
- Devices and Circuit Measurements
- Low Noise Circuit Design for Sensor Interface
- Analog Integrated Circuits and Signal Processing
- PDK Benchmarking - Testing, CMOS/SiGe BiCMOS/SOS, FinFET processes
- Semiconductor Technology, Compact Modeling/Noise Modeling and Simulation (publications list)
- Digital Circuits (CAD)-Computer Architecture, FPGA, Microcontrollers (preliminary)

Electronic Design Automation & Measurement Automation Tools
- Cadence Suite, HSPICE-PSPICE, Spectre
- Modelsim, Aldec Active–HDL, Mentor Leonardo Spectrum
- ICCAP, Agilent – Momentum, HFSS

Hardware Description Languages
- VHDL, Verilog, Assembly (preliminary), SKILL, UNIX Scripting

Continuous Training – Knowledge Certification

- "Cadence *Spectre RF*", October 24-25, 2013, Intel Mobile Com. Austria, Villach Innovation Design Center - Austria
- "*Career Development in ICs",* INTEL Training Center, August 26, 2013, Neubiberg, Germany.
- "*Cadence SKILL programming Language*", EMEA Cadence Training Center, August 19-23, 2013, Feldkirchen-Munich, Germany.
- "*Cadence Virtuoso Spectre Circuit Simulator MMSIM 10.1 (Custom IC Design – Virtuoso)",* EMEA Cadence Training Center, October 9-11, 2012, Feldkirchen-Munich, Germany.
- "*c14nm Design Environment for Analog/RFMS Design"* Intel TMG "in-house" Training – *RV simulation, Self-heating effect simulation, Genesis and Genoa Design Env* - August 2012, Hillsboro, Oregon - US.
- *"IC-CAP (Integrated Circuits Characterization and Analysis Program) Learning Week*", Boeblingen (Stuttgart Area), Germany, June 11-15, 2012, Agilent Technologies, EEsof EDA Europe.
- *"Decision making using RAPID, IP Control protocol, product development security, protecting classified information, Deemed exports- & exports control basics – global export compliance, information classification and privacy essentials" Intel 'in-house training series'*– June 2012, Intel Mobile Communications GmbH, Munich Area-Germany
- *"Advanced Analog Implementation flow : Analog circuit design simulation and layout for 90nm and below*", Thessaloniki, Greece, January 19-23, 2009 (organized by Europractise)

International Conferences

- Chairman in the session "Analog and High Frequency RF Electronic Circuits" / Poster presentation - Participation in the "2nd Pan-Hellenic conference on Electronics and Telecommunications", Thessaloniki 16-18, 2012.
- Participation in the 2009 Topical Workshop for Electronics for Particle Physics (TWEPP) – Organized by CERN, Paris, France, September 21-25, 2009 (1 poster presentation)

- Participation in the 2008 Topical Workshop for Electronics for Particle Physics (TWEPP) – Organized by CERN, Naxos, Greece, September 15-19, 2008 (2 poster presentations)
- Speaker in the 2nd IEEE Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Otranto (Lecce), Italy, June 12-15, 2006 (2 oral presentations)
- Participation in the 2nd Conference on Microelectronics, Microsystems and Nanotechnology (MMN), Athens, Greece, November 14-17, 2004 (1 poster presentation)
- Speaker in the 12th IEEE Mediterranean Electro-technical Conference (MELECON), Dubrovnik, Croatia, May 12-15, 2004 (1 oral presentation)

Research Activity

A. Scientific Publications

I. Book Editing

E1. T. Noulis, "Mixed Signal Circuits" in the series "Devices, Circuits and Systems", Invited by CRC Press 2015 - to be published – Dec.2015.

II. Patents

P1. *Patent (WO2010/084280A1)* on radiation detection electronics (French Patent & PCT application) entitled: *"Amplification structure and detection and measurement sequence comprising such a structure"*, Inventors: Thomas Noulis, Stylianos Siskos, Gerard Sarrabayrouse, Laurent Bary.

P2. Brevet d 'inventione 'n France, "Structure d'amplification et chaine de detection et de mesure comportant une telle structure", Inventors: Thomas Noulis, Stylianos Siskos, Gerard Sarrabayrouse, Laurent Bary.

III. Publications in Semiconductor Industry Workshops

D1. "*A Substrate Noise Analysis and RLCK Extraction Flow for RF & High-Speed Design*" – HELIC Inc. presentation - 1st TSMC Open Innovation Platform Ecosystem Forum, October 18th, 2011 in San Jose Convention Centre, CA, USA

VI. Publications in International Scientific Journals

J1. T. Noulis, S. Siskos, G. Sarrabayrouse, *Noise Optimized Charge Sensitive CMOS amplifier for Capacitive Radiation Detectors,* IET Circuits Devices and Systems, vol 2, Issue 3, pp. 324-334, June 2008.
J2. T. Noulis, C. Deradonis, S. Siskos, G. Sarrabayrouse, *Particle detector tunable monolithic semi-gaussian shaping filter based on Transconductance amplifiers,* Nuclear Instruments and Methods in Physics Research A vol. 589, pp.330-337, 2008.
J3. T. Noulis, S. Siskos, G. Sarrabayrouse, L. Bary, *Advanced Low Noise X-ray readout ASIC for Radiation Sensor Interfaces,* IEEE Trans. Circuits and Systems, Part 1, vol.55, no.7 August 2008.
J4. T. Noulis, S. Siskos, G. Sarrabayrouse *Analysis and selection criteria of BSIM4 flicker noise simulation models,* International Journal of Circuit Theory and Applications, vol.36, pp.813–823, 2008.
J5. T. Noulis, C. Deradonis, S. Siskos, *Design Guidelines and Comparison of Detector Readout Front end integrated S-G Shapers using Transconductance circuits*, International Journal of Electronics, vol. 94, No.10, pp. 943-959, 2007.
J6. T. Noulis, C. Deradonis, S. Siskos, G. Sarrabayrouse, *Detailed Study of Particle detectors OTA based CMOS Semi-Gaussian Shapers*, Nuclear Instruments and Methods in Physics Research A, vol. 583, pp.469-478, 2007.
J7. T. Noulis, C. Deradonis, S. Siskos, *Advanced Readout System IC Current Mode Semi-Gaussian Shapers Using CCIIs and OTAs*, VLSI Design Journal, vol. 2007, article ID. 71684, 2007.
J8. T. Noulis, S. Siskos, G. Sarrabayrouse, *Comparison between BSIM4.X and HSPICE flicker Noise Models in NMOS and PMOS transistors in all Operating Regions*, Microelectronics Reliability, vol. 47, pp.1222-1227, 2007.

V. Publications in Conferences & Workshops

C1. A. Voulkidou, S. Siskos, T. Noulis, "Simulation Inaccuracies in Analog/RF Integrated Circuit Design in CMOS Process", PACET - 2nd Pan-Hellenic conference on Electronics and Telecommunications, March 16-18, 2012, Thessaloniki - Greece
C2. T. Noulis, A. Voulkidou, S. Siskos, G. Sarrabayrouse, *"Current Mode Low BW - Large Peaking Time CMOS S-G Shaper Using CA Building Cells"*, IEEE 15th Mediterranean Electrotechnical Conference (MELECON 2010) - Proceedings, Valletta, Malta, April 26-28, 2010.
C3. T. Noulis, N. Kaiserlis, S. Siskos, G. Sarrabayrouse, *" SiGe BiCMOS CSA-Shaper Radiation Detection Front End: Noise Performance and Noise Modelling"*, IEEE 15th Mediterranean Electrotechnical Conference (MELECON 2010) - Proceedings, Valletta, Malta, April 26-28, 2010.
C4. T. Noulis, S. Siskos, G. Sarrabayrouse, L. Bary, *Novel charge sensitive amplifier design methodology suitable for large detector capacitance applications*, Topical Workshop on Electronics for Particle Physics 2009 (TWEPP 2009, by CERN), Paris, France, September 21-25, 2009.
C5. T. Noulis, S. Siskos, G .Sarrabayrouse, L. Bary *Current mode Charge Sensitive Amplifying Technique providing Noise Performance Independent of the Radiation Detector Capacitance,* 3rd IEEE International Workshop on Advances in Sensors and Interfaces (IWASI 2009) , Trani (Bari), Italy, June 25-26, 2009.
C6. T. Noulis, G. Fikos, S. Siskos, G. Sarrabayrouse, *Folded Cascode Amplifying structure evaluation in terms of the used IC process in Radiation Detection front End applications*, 1st international conference on Technology and Instrumentation in Particle Physics (TIPP 2009), Epocal Tsukuba, Tsukuba, Japan, March 12-19, 2009.
C7. T. Noulis, V. Kalenteridis, S. Siskos and G. Sarrabayrouse, *Radiation Detection Low Frequency CMOS S-G Shaper using Transconductance Circuits*, 1st international conference on Technology and Instrumentation in Particle Physics (TIPP 2009), Epocal Tsukuba, Tsukuba, Japan, March 12-19, 2009.
C8. T. Noulis, G. Fikos. S. Siskos, G .Sarrabayrouse, *Noise analysis of Radiation Detector Charge Sensitive Amplifier Architectures*, Topical Workshop on Electronics for Particle Physics 2008 (TWEPP 2008, by CERN), Naxos, Greece, September 15-19, 2008.

C9. T. Noulis, S. Siskos, G .Sarrabayrouse, *Development and Testing of an Advanced CMOS Readout Architecture dedicated to X-rays silicon strip detectors*, Topical Workshop on Electronics for Particle Physics 2008 (TWEPP 2008, by CERN), Naxos, Greece, September 15-19, 2008.
C10. T. Noulis, S. Siskos, L. Bary, G .Sarrabayrouse, *Non Inverting Voltage Amplifier noise analysis using a CCII∞ based structure*, 16th IFIP/IEEE SOCVLSI 2008, Rhodes island, Greece, October 13-15, 2008.
C11. T. Noulis, S. Siskos, G .Sarrabayrouse, *Noise Performance of Current and Voltage Mode CMOS Preamplifiers for X-rays Detection Systems*,21st Conference on Design of Circuits and Integrated Systems (DCIS 2006),Barcelona, Spain, November 22-24, 2006.
C12. T. Noulis, S. Siskos, *A Space Application Current Mode CMOS Low Noise Preamplifier for X-rays Detection Systems,* XLI International Scientific Conference on Information,Communication and Energy Systems and Technologies (ICEST 2006), Sofia, Bulgaria, June 29- July 1, 2006.
C13. T. Noulis, C. Deradonis, S. Siskos, *Current mode CMOS OTA based Band Pass Filters for Detector Readout Front Ends*, XLI International Scientific Conference on Information, Communication and Energy Systems and Technologies (ICEST 2006), Sofia, Bulgaria, June 29- July 1, 2006.
C14. T. Noulis, C. Deradonis, S. Siskos, G. Sarrabayrouse, *Analysis of OTA based Semi Gaussian Design Techniques for Low Energy X-rays Detection Systems*, 7th International Workshop on Low Temperature Electronics (WOLTE 2006 by ESA), Workshop - Proceedings, Noordwijk-ESA, The Netherlands, June 21-23, 2006.
C15. T. Noulis, C. Deradonis, S. Siskos, *Design and Comparison o f CMOS CCII based Shapers for Detector Readout Front Ends*, IEEE 2nd Conference on PhD Research in Microelectronics and Electronics (PRIME 2006), Conference - Proceedings, Otranto, Italy, June 11-15, 2006.
C16. T. Noulis, C. Deradonis, S. Siskos, G. Sarrabayrouse, *Programmable OTA based Shaping Amplifier for X-rays Spectroscopy*, IEEE 2nd Conference on PhD Research in Microelectronics and Electronics (PRIME 2006), Conference - Proceedings, Otranto, Italy, June 11-15, 2006.
C17. T. Noulis, C. Deradonis, S. Siskos, G. Sarrabayrouse, *Novel Fully Integrated OTA based Front End Analog Processor for X-rays Silicon Strip Detectors*, IEEE 13th Mediterranean Electrotechnical Conference (MELECON 2006) - Proceedings, Malaga, Spain, May 16-19, 2006.
C18. T. Noulis, S. Siskos, G. Sarrabayrouse, L. Bary and A. A. Hatzopoulos, *Detailed Study of BSIM3v3 Flicker Noise Models in NMOS and PMOS Transistors from Threshold to Saturation*, 20th Conference on Design of Circuits and Integrated Systems (DCIS 2005), Lisboa, Portugal, November 23-25, 2005.
C19. T. Noulis, M. Drakaki, S. Siskos, *Complete Analysis of BSIM3 noise models for the optimum design of a low noise preamplifier*, 2nd Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004), Athens, Greece, November 14-17, 2004.
C20. T. Noulis, S. Siskos, G. Sarrabayrouse, *Analysis of Input and Feedback Capacitances Effect on Low Noise Preamplifier Performance for X-rays Silicon Strip Detectors*, 19th Conference on Design of Circuits and Integrated Systems (DCIS 2004), Bordeaux, France, November 24-26, 2004.
C21. T. Noulis, S. Siskos, G. Sarrabayrouse, *Effect of Technology on the input Transistor Selection Criteria of a Low Noise Preamplifier*, IEEE 12th Mediterranean Electrotechnical Conference (MELECON 2004) - Proceedings, Dubrovnik, Croatia, May 12-15, 2004.

IV. Book Chapters

B1. T. Noulis, "Integrated Analog Signal Processing Readout front Ends for Particle detectors", *invited* for publication in the book 'Materials for Radiation Detection', editors, Patrick Doty and Kris Iniewski, CRC Press 2014.
B2. T. Noulis, S. Siskos, L. Bary, G. Sarrabayrouse *"Discussion on 1/f noise in CMOS transistors: Modelling-simulation and measurement techniques"* Chapter 10 in the Book "MOSFETs: Properties, Preparations and Performance", *Invited* by NOVA Science Publishers, Inc., 4th Quarter 2008/ Chapter 8 in the Book "CMOS technology", NOVA Science Publishers, Inc., 2nd Quarter 2010.
B3. T. Noulis, *"MOSFET modeling: Reliability and Validation for Analog/RF IC design"* – Chapter 5 in the Book "CMOS technology" (*invited*), NOVA Science Publishers, Inc., 2nd Quarter 2010

V. Publications in Special Issues

D1. T. Noulis, M. Drakaki, S. Siskos, *"Complete Analysis of BSIM3 noise models for the optimum design of a low noise preamplifier"*, Published in the Journal of Physics: Conference Series v.10.

C. Services

Reviewer in international journals
- IET Electronic Letters (IET)
- IEEE Transactions on Instrumentation & Measurement (IEEE),
- Nuclear Instruments and Methods in Physics Research A (Elsevier)
- Circuits and Systems for signal Processing (Springer)
- International Journal of Circuit Theory and Applications (Wiley)
- Microelectronics Journal (Elsevier)
- Materials Science in Semiconductor Processing (Elsevier)

Reviewer in international conferences
- IEEE : MELECON 2006SOCVLSI 2008, , ICECS 2010, NEWCAS 2015,
- Non IEEE : DCIS 2006

Honors, Awards & Citations

- Grant Award (funding) in the framework of the Marie Curie 2009 ACEOLE action as promising young researcher to participate to the 2009 Topical Workshop on Electronics for Particle Physics (TWEPP09), September 2009, Paris–France organized by CERN

- Aristotle Univ. Research committee Honors Scholarship for the year 2008, 1st place (award) between the Physics Dept. PhD candidates (June 2008)
- 1st place and corresponding award from the Greek State Scholarship's Foundation after the completion of 2 years studies at the Master Degree Program on Electronic Physics at the Physics Dept. of Aristotle University of Thessaloniki, Greece for the academic year 2004-2005 (September 2005)
- IEEE MELECON 2004 *Best Student Paper Award* in the area of Circuits and Systems for Signal Processing, for the paper "*Effect of Technology on the input Transistor Selection Criteria of a Low Noise Preamplifier*", (T. Noulis, S. Siskos, G. Sarrabayrouse) - May 2004
- Over 50 citations in journal and conferences papers, patents and books to the research work

Invited Lectures

- Invited presentation on "Mixed Signal SoC Substrate Coupling" at MOCAST 2015 - The International Conference on Modern Circuits and Systems Technologies (MOCAST) - 14 - 15 May 2015 Thessaloniki Greece
- Invited presentation on "SoC substrate crosstalk and EDA tools challenges" at "Pan-Hellenic Conference on Electronics and Telecommunications - PACET "- Πανελλήνιο Συνέδριο Ηλεκτρονικής και Τηλεπικοινωνιών – 8 and 9/5 , Ioannina, Greece
- Invited Lectures on "Mixed Signal SoC Substrate Coupling and EDA limitations" at Laboratoire d'Analyse et d'Architecture des Système, Seminaire de l'equipe N2IS, (LAAS) – CNRS , Sept.20-21, 2012, Toulouse, France.
- Invited Speaker at the Physikalisches Institut, Universitaet Bonn, Germany - "Readout front Front-end ICs" in Scientific Seminars – January 2009
- Lecture on "Radiation detection ICs" at the Paul Sherrer Institute (PSI), Villigen (Brugg), Switzerland - May 2008

Spoken Languages

- English, Excellent knowledge (Certificate Proficiency in English)
- German, Elementary Knowledge (Berlitz Deutsch Sprachschulen level 4)
- Greek , Native

Interests – Hobbies

- Music (Experienced Violinist (15 years studies- diploma) and Pianist)
- Mountain Bike, Hiking, Jogging

References Available on demand