Curriculum Vitae

Dr. Ilias N. Pappas

Personal Data

Date of birth	31/07/1980
Place of birth	Ioannina, Ioanninon
Family status	Married (one child)
Home address	Filippou 43B 55535, Pilaia, Thessaloniki Greece
Work address	Physics Department, Electronics Lab. Aristotle University of Thessaloniki 54124, Thessaloniki Greece
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Occupation

Physicist – M.Sc. and Dr. in Electronics Engineering

Education

April 2006 – December 2009 **Ph.D Dissertation on the "**Development of polycrystalline silicon thin-film transistor models for SPICE – like circuit simulation – Circuit design implemented with TFTs**",** Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki, Greece.
CGPA: Excellent

2002-2005 **M.Sc. Diploma in Electronic Physics - Radioelectronics,**
(Option: Technology of Electronic Circuits) Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki,
CGPA: 8.97/10 (Excellent)

1998-2002 **B.Sc. Degree in Physics** (Option: Electronics & Telecommunications),
Physics Department , Aristotle University of Thessaloniki,
CGPA: 7.35/10 (Very Good)

Professional and Research Experience

March 2010 – December 2010 (plus year 2011)

Participation to the Greek Ministry of Development and EU funded research project MEMSENSE (code number: 84009): "MEMSENSE: Next generation of smart MEM sensors".

Position: Primary researcher
Project Duration: 10 months (and 2011)

Description: Study and design of read-out and peripheral analog circuits for smart sensors (temperature, pressure, air flow, acceleration). Circuit design for energy harvesting.

1st November 2006 - 30th October 2007	National Polytechnic Institute of Grenoble (INPG), France Laboratory IMEP (Institute of Microelectronics Electromagnetic and Photonics) **Position**: Researcher **Duration** : 1 year **EU Program:** Human Resources and Mobility - Marie Curie Action (RTN, EST and SCF). **Description**: *ST Microelectronics Framework – PULLNANO Consortium.* Research deals with the study, measurements, characterization and modeling of nano-scale (below 0.45 μm) advanced CMOS technologies like Full-Depleted Silicon On Insulator (FD-SOI) devices and Silicon On Nothing (SON) devices.
April 2004 - September 2006	Participation to the Greek Ministry of Education funded research project PYTHAGORAS (code number: 21901): "PYTHAGORAS: Study and Development of Thin-Film Transistors models-Circuit Design by using TFTs-Design and Development of accumulators of Li ions for their supply". **Position:** Primary researcher **Project Duration**: 32 months **Description:** Study and development of new poly-Si TFT's models and analog circuits design for Liquid Crystal Display arrays by using poly-Si TFTs.
September 2002 - February 2004	Participation to the EU funded research project IST-2001-34379: "Architectures and Methodologies for Dynamic Reconfigurable Logic (AMDREL)". **Position**: Researcher of AUTH team **Project Duration**: 18 months **Description**: Full custom implementation of a low power Field-Programmable Gate Array (FPGA). Primary designer of the circuit design of the chip. Responsible for low power techniques, design of main components and the memory unit. Contribute to the FPGA's architecture and the layout design of the chip.

Relevant Skills

- Design of voltage / current – programmed pixels for AMOLED displays application (see publications).
- Design of voltage / current driving circuits for flat panel displays (see publications).
- Compact modeling of thin-film and SOI transistors (see publications).
- Transistor measurements (I – V electrostatic, capacitance, thermo – cryo, dynamic transconductance, AC / DC stress, noise).
- Transistor parameters extraction.
- FGMOS circuit design.
- Full custom design of digital block (FPGA application) with low power techniques (see publications).
- Digital Circuits (CAD) - Computer Architecture, FPGA, Microcontrollers

Electronic Design Automation Tools

- SPICE (P - H – AIM - Spice), Cadence Suite, Electronic Workbench,
- Modelsim, Aldec Active–HDL, Mentor Leonardo Spectrum (elementary)
- Silvaco tools for transistor modelling (ATLAS, ATHENA, MIXMODE)

Application Development Tools

- Mathematica, Mathcad, Matlab (elementary)

Hardware Description Languages

- VHDL, Assembly (elementary)

Office Automation/Other

- MS Office-Open Office, MS Visio, Microcal Origin, Open workbench

Operation Platforms

- Ms Windows 98/2000/XP/Vista/7
- Linux (Fedora 9), Unix (Sun – Solaris)

International Conferences / Seminars / Summer Schools

May 2010	2010 International Symposium of Society for Information Display, SID Week Event, 24-28 May, Seattle, WA, USA. (poster presentation).
December 2009	16th IEEE International Conference on Electronics Circuits and Systems (ICECS 2009), Hammamet 13-16 December, Tunisia, 2009. (oral presentation)
November 2007	XXII Conference on Design of Circuits and Integrated Systems (DCIS 2007), 21-24 November, Sevilla, Spain. (oral presentation).
June 2007	MIGAS Summer School 2007 Topic: Multi – Physics and Multi – Scale Simulation for Nano – Electronics 24 – 29 June, Autrans – Grenoble, France Duration: 80 hours
May 2006	25th International Conference on Microelectronics, MIEL 2006, 14-17 May, Belgrade, Serbia and Montenegro. (poster presentation)
November 2004	2nd Conference on Microelectronics, Microsystems and Nanotechnology MMN 2004, November 14-17, 2004, Athens, Greece. (poster presentation)
October 2003	**"**Design of Low-Power Digital Circuits: Techniques and Tools" at Athens Information Technology, Athens, Greece, Instructors from Politecnico di Torino and BullDAST, Italy.

Research Activity

A. Publications in International Journals

1. **I. Pappas**, S. Siskos and C. A. Dimitriadis, "Polycrystalline Silicon TFTs Threshold Voltage Compensated Transconductor for Analog Circuit Design", accepted for publication in *IEEE Journal of Display Technology.*
2. **I. Pappas**, S. Siskos and C. A. Dimitriadis, "A New Threshold Voltage Compensation Technique of poly-Si TFTs for AMOLED Displays Pixel Circuits", *Journal of the Society for Information Display*, vol. 18, p.p. 721 – 731, October 2010.
3. **I. Pappas**, G. Ghibaudo, C. A. Dimitridis and C. Fenouillet-Béranger, "Backscattering Coefficient and Drift – Diffusion Mobiltiy Extraction in Short Channel MOS Devices", *Elsevier Journal of Solid – State Electronics*, vol. 53, p.p. 54-56, January 2009.
4. **I. Pappas,** S. Siskos, G. Ghibaudo and C. A. Dimitriadis, "Comparison of two analog buffers implemented with low-temperature polysilicon thin-film transistors for Active Matrix Display applications", *Journal of Physica Status Solidi,* vol. 5, No. 12, p.p. 3854 – 3857, September 2008.
5. **I. Pappas,** C. A. Dimitriadis, S. Siskos, F. Templier, M. Oudwan and G. Kamarinos, "Effect of Channel Width Shortening on the Stability of a-Si:H/nc-Si:H Bilayer Thin-Film Transistors", *IEEE Electron Device Letters*, vol. 29, No. 8, August 2008, p.p. 871 - 873.
6. **I. Pappas,** S. Siskos and C. A. Dimitriadis, "A Fast and Compact Analog Buffer Design for Active Matrix Liquid Crystal Displays Using Polysilicon Thin-Film Transistors", *IEEE Transactions on Circuits and System II: Express Briefs,* vol. 55, No. 6, June 2008, p.p. 537 -540 .
7. **I. Pappas,** C. A. Dimitriadis, F. Templier, M. Oudwan and G. Kamarinos, "Above-threshold drain current model including band tail states in nanocrystalline silicon thin-film transistors for circuit implementation", *Journal of Applied Physics*, vol. 101, Art. No. 084506, April 2007.
8. **I. Pappas,** S. Siskos and C. A. Dimitriadis, "A New Analog Buffer Using Low-Temperature Polysillicon Thin-Film Transistors for Active Matrix Displays", *IEEE Transactions of Electron Devices,* vol 54, No 2, p.p. 219-224, February 2007 .
9. A. T. Hatzopoulos, **I. Pappas**, D. H. Tassis, N. Arpatzanis, C. A. Dimitriadis, F. Templier and M. Oudwan, "Analytical current – voltage model for nanocrystalline silicon thin-film transistors", *Applied Physics Letters,* vol 89, Art. No. 193504, November 2006. (cited: 4 times).

10. **I. Pappas,** A. T. Hatzopoulos, D. H. Tassis, N. Arpatzanis, S. Siskos and C. A. Dimitriadis, " A simple and continuous polycrystalline silicon thin-film transistor model for SPICE implementation", *Journal of Applied Physics,* vol 100, 064506, September 2006.

11. V. Kalenteridis, H. Pournara, K. Siozos, K. Tatas, N. Vassiliadis, **I. Pappas**, G. Koutroumpezis, S. Nikolaidis, S. Siskos, D.J. Soudris and A. Thanailakis, "A complete platform and toolset for system implementation on fine-grain reconfigurable hardware", Elsevier Microprocessors and Microsystems, Volume 29, Issue 6, 11 August 2005, Pages 247-259.

12. K. Siozios, G. Koutroumpezis, K. Tatas, N. Vassiliadis, V. Kalenteridis, H. Pournara, **I**. **Pappas**, D. Soudris, A. Thanailakis, S. Nikolaidis, S. Siskos "A Novel FPGA Architecture and an Integrated Framework of CAD Tools for Implementing Applications", Special Section on Recent Advances in Circuits and Systems- Part 1, IEICE Trans. on Information and Systems, vol. E88-D, No. 7, July 2005, p.p 1369-1380.

B. Publications in International Conferences

1. **I. Pappas,** D. Tassis, S. Siskos and C. A. Dimitriadis, "Characteristics of Double-Gate Polycrystalline Silicon Thin-Film Transistors for AMOLED Pixel Design", accepted for publication in ICECS 2010 Conference, held in Athens, 12-15 December 2010.

2. **I. Pappas**, S. Siskos, G. Theodoratos and M. Zervakis, "A New Over-Current Protection Architecture for Low Drop Out Regulator Applications", accepted for publication in MMN 2010 Conference.

3. **I. Pappas**, S. Siskos and C. A. Dimitriadis, "A New Threshold Voltage Compensation Technique of poly-Si TFTs for AMOLED Displays Pixel Circuits", in Proceeding of SID 10 Digest, SID International Symposium on Displays – Proceeding, SID Display Week 2010 , pp. 1336 – 1339, Seattle, Washington, USA, May 23 -28, 2010.

4. **I. Pappas**, C. Theodorou, S. Siskos and C.A. Dimitriadi, "A New Linear Voltage-to-Current Converter With Threshold Voltage Compensation for Analog Circuits Applications in Polycrystalline Silicon TFT Process", in Proceedings of 16th IEEE International Conference on Electronics Circuits and Systems (ICECS 2009), Hammamet 13-16 December, Tunisia, 2009.

5. **I. Pappas**, S. Siskos, G. Ghibaudo and C. A. Dimitriadis, "A New Topology of Analogue Buffer Using Low-Temperature Polysilicon Thin-Film Transistors for Liquid Crystal Displays Applications", in Proceedings of XXII Conference on Design of Circuits and Integrated Systems (DCIS 2007), 21 – 23 November 2007, Seville, Spain.

6. **I. Pappas**. S. Siskos, G. Ghibaudo and C. A. Dimitriadis, "A Comparison of Two Analogue Buffers, Implemented with Low-Temperature Polysilicon Thin-Film Transistors, for Active Matrix Displays Applications", in Proceedings of Third International Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2007), 18-21 November 2007, Athens, Greece.

7. N. P. Papadopoulos, A. A. Hatzopoulos, **I. Pappas**, D. K. Papakostas, C. A. Dimitriadis and S. Siskos, "Spice Model for the simulation of the Light impact on the performance of polycrystalline Thin-Film Transistors", in Proceedings of XXI Conference on Design of Circuits and Integrated Systems (DCIS 2006), Barcelona 22 – 24 November 2006.

8. **I. Pappas**, L. Nalpantidis, V. Kalenteridis, S. Siskos, C.A. Dimitriadis and A. A. Hatzopoulos, "A Threshold Voltage Variation Cancellation Technique for Analogue Peripheral Circuits of a Display Array Using Polysilicon TFTs," 2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006), p.p. 3305-3308, 21-24 May 2006, Kos, Greece.

9. **I. Pappas**, A. T. Hatzopoulos, D. H. Tassis, N. Arpatzanis, S. Siskos, A.A. Hatzopoulos, C. A. Dimitriadis and G. Kamarinos, "A Simple Polysilicon Thin-Film Transistor SPICE Model", in Proceedings of 25th International Conference on Microelectronics (MIEL 2006), p.p. 513-516, 14-17 May 2006, Belgrade, Serbia and Montenegro.

10. **I. Pappas**, L.Nalpantidis, V.Kalenteridis, S.Siskos, A.A. Hatzopoulos, C.A. Dimitriadis, "A new analogue driver using Poly-Si Thin-Film Transistors for Active Matrix Displays", in Proceedings of XX Conference on Design of Circuits and Integrated Systems (DCIS 2005), November 25-27, Lisboan, Portugal.

11. A.A Hatzopoulos, S.Siskos, C.A. Dimitriadis, N. Papadopoulos, **I. Pappas**, L. Nalpantidis, 'Built-In Current Sensor using thin-film transistor', Journal of Physics: Conference Series, Volume 10, 2005, p.p. 289-293, 2nd Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004), 14-17 November 2004, Athens, Greece.

12. **I. Pappas**, L.Nalpantidis, V.Kalenteridis, S.Siskos, C.A.Dimitriadis, "A study of different types of current mirrors using Polysilicon TFTs", Journal of Physics: Conference Series, Volume 10, 2005, p.p. 373-377. 2nd Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004), 14-17 November 2004, Athens, Greece.

13. **I. Pappas**, V.Kalenteridis, N.Vassiliadis, H.Pournara, K.Siozios, G.Koutroumpezis, K.Tatas, S.Nikolaidis, S.Siskos, D.J.Soudris, and A.Thanailakis, "Fine-Grain Reconfigurable Platform: FPGA Hardware Design and Software Toolset Development Journal of Physics: Conference Series, Volume 10, 2005, p.p. 352-357, 2nd Conference on Microelectronics, Microsystems and Nanotechnology (MMN 2004), 14-17 November 2004, Athens, Greece.

14. K. Siozios, G. Koutroumpezis K. Tatas, N. Vassiliadis, H. Pournara**, I. Pappas**, D. J. Soudris, S. Nikolaidis, S. Siskos, V. Kalenteridis, A. Thanailakis "AMDREL: Project in retrospective", IFIP Int. Conf. in Very Large Integration VLSI-SOC, October 17-19, 2005, Perth, Australia.

15. D. Soudris, S.Nikolaidis, S.Siskos, K.Tatas, K.Siozios, G.Koutroumpezis, N.Vassiliadis, V.Kalenteridis, H.Pournara, **I. Pappas**, and A.Thanailakis, "AMDREL: A novel low-energy FPGA architecture and supporting cad tool design flow", Asia and South Pacific Design Automation Conference 2005 (ASP-DAC 2005), 18 – 21 January 2005, Shanghai, China.

16. H.Pournara, V.Kalenteridis, **I.Pappas**, N.Vassiliadis, S.Nikolaidis, S.Siskos, and D.J.Soudris, "Energy Efficient Fine-Grain Reconfigurable Hardware", in Proceedings of 12th IEEE Mediterranean Electrotechnical Conference (MELECON 2004), 12 - 15 May 2004, Dubrovnik, Croatia.

17. V.Kalenteridis, H. Pournara, K. Siozios, K. Tatas, **I. Pappas**, N. Vassiliadis, G. Koutroumpezis, S. Nikolaidis, S.Siskos, D. J. Soudris and A. Thanailakis "An Integrated FPGA Design Framework: Custom Designed FPGA Platform and Application Mapping Toolset Development", in Proceedings of the 11th Reconfigurable Architectures Workshop (RAW 2003) 26-27 April 2003, Santa Fe, New Mexico, USA.

C. Patent

1. "Display element, display using the same and driving method for the same", Patent submitted in the European Patent Office (Patent No. : 09157123.2-1228, Date: 01/04/2009). Inventors: **I. Pappas**, S. Siskos and C. A. Dimitriadis.

D. Book Chapters

1. D. Soudris, K. Tatas, K. Siozios, G. Koutroumpezis, S. Nikolaidis, S. Siskos, N. Vasiliadis, V. Kalenteridis, H. Pournara and **I. Pappas**. Chapter 3: "AMDREL: A Novel Low-Energy FPGA Architecture and Supporting CAD Tool Design". Book: "Fine and Coarse-Grain Reconfigurable Computing: Architectures, Processors, Case Studies", pp. 153 – 180, Springer Publishers, ISBN: 978-1-4020-6504-0.

2. **I. Pappas,** S. Siskos, C. A. Dimitriadis, Chapter 8: "Active-Matrix Liquid Crystal Displays – Operation, Electronics and Analog Circuit Design", book title: "New Developments in Liquid Crystals", pp. 147 – 170, In-Tech Publisher. ISBN: 978-953-307-015-5.

F. Services

Reviewer for International:

1 ***Journals:*** *IEEE Transaction on Electron Devices, IEEE Electron Devices Letters, IEEE Sensors, Journal of SID, IOP Semiconductor Science Technology, IEEE Journal of Display Technology .*

2 ***Conferences:*** *IFIP/IEEE VLSI-SOC 2008, ICECS 2010.*

Languages

Greek	Native
English	First Certificate**,** excellent technical knowledge

Awards – Others

May 2010	Student Grant Award (travelling funds) to participate to the 2010 Display Week Event and 2010 Society for Information Displays International Conference, 23 – 28 May, Seattle – Washington, USA organized by Society for Information Displays (SID).

September 2006	1 year Research Grant, funded by EU Program: Human Resources and Mobility - Marie Curie Action (RTN, EST and SCF). Constitution: IMEP laboratory, Minatec, INP Grenoble, France.
January 2005	Honourable mention for design contest entry for the design "AMDREL: A novel low-energy FPGA architecture and supporting CAD tool design flow" VLSI Design Contest, January 2005, Taj Bengal, Kolkata, India.

24 citations to the research work

Interests – Hobbies

- Sports (volleyball, football and basketball)
- Travelling
- Music

References Available on demand